PROMs/ROMs

MM4240/MM5240 2560-bit static character generator

general description

The MM4240/MM5240 2560-bit static character generator is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology. Six character address and three row address input lines provide access to 64–8 x 5 characters. Customer-generated single or multiple package character fonts are easily programmed by completing a pattern selection form. A standard 7 x 5 raster scan font is available by ordering the MM4240AA/MM5240AA.

The MM4240/MM5240 may be used as a 512 x 5-bit read only memory for applications other than character generation.

features

- Bipolar compatibility
- High speed operation—500 ns max
- ±12 volt power supplies
- Static operation—no clocks required
- Multiple ROM logic application—chip enable output control
- Standard fonts available—off-the-shelf delivery

applications

- Character generation
- Random logic synthesis
- Microprogramming
- Table look-up

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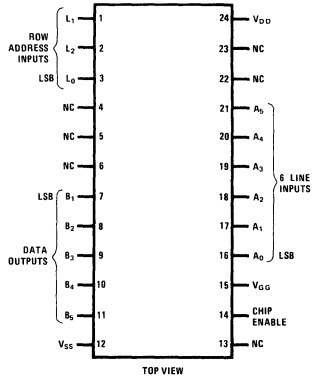
connection diagram

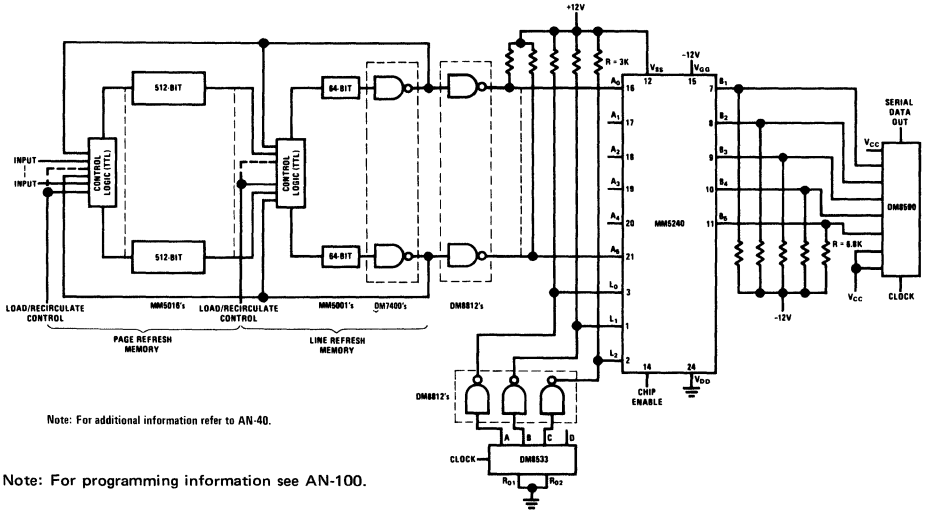
Dual-In-Line Package



TOP VIEW

Order Number MM4240J
or MM5240J
See Package 11
Order Number MM5240N
See Package 18

typical application



Note: For additional information refer to AN-40.

Note: For programming information see AN-100.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} – 30V
V_{DD} Supply Voltage		V_{SS} – 15V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		–65°C to +150°C
Operating Temperature	MM4240	–55°C to +125°C
	MM5240	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	IMΩ to GND			V_{SS} – 9.0	V
Logical "0"		V_{SS} – 1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.5			V
Output Current Capability					
Logical "0"	$V_{OUT} = V_{SS} - 6.0V$	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 8.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	$T_A = 25°C$				
I_{DD}	MOS Load		25	40	mA
I_{GG} (Note 2)				1	μA
Input Leakage	$V_{IN} = V_{SS} - 12V$			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		5	8	pF
V_{GG} Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		25	40	pF
Address Time (Note 3)	See Timing Diagram				
T_{ACCESS}	$T_A = 25°C$	150	425	500	ns
Output AND Connection	MOS Load			4	
(Note 4)	TTL Load			10	

Note 1: These specifications apply for V_{SS} = +12V ±5%, V_{GG} = –12V ±5%, and T_A = –55°C to +125°C (MM4240) T_A = 0°C to +70°C (MM5240) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns

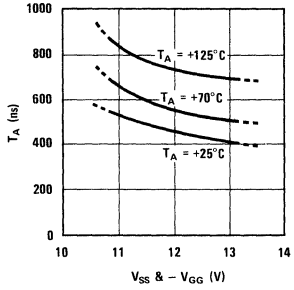
Where N = Number of AND connections.

The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

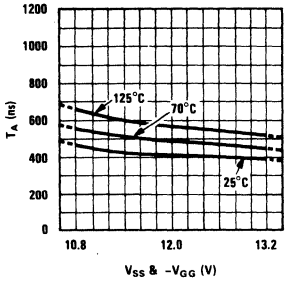
Note 5: Guaranteed by design.

performance characteristics

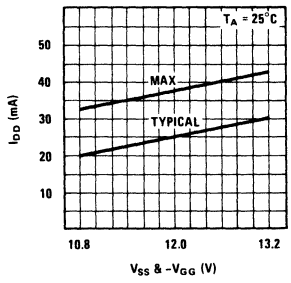
Guaranteed Access Time (T_A) vs Supply Voltage



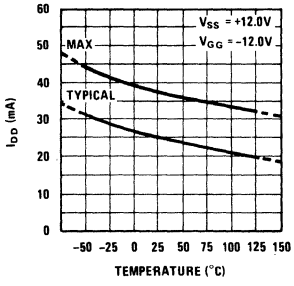
Typical Access Time (T_A) vs Supply Voltage



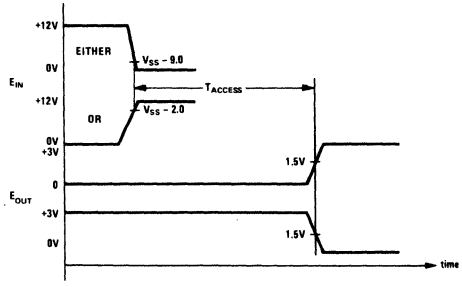
Power Supply Current vs Voltage

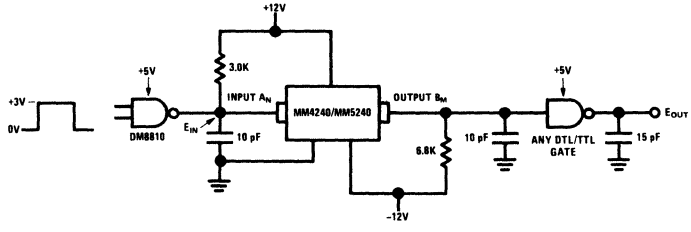


V_{DD} Power Supply Current vs Temperature



timing diagram/address time





MM4240AA/MM5240AA character font