S/50™ Reference Manual

Convergent Technologies

S/5Ø Hardware Reference

First Edition (November 1986) Ø9-Ø13Ø7-Ø1

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WARNING

This equipment has been certified to comply with the limits for a Class B computing device, pursuant to Subpart J of Part 15 of FCC Rules. Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this computer, when installed in a residential environment. Operation with peripherals that are not certified to comply with Class B Subpart J of Part 15 of FCC Rules is likely to result in interference to radio and TV reception, if installed in a residential environment.

When this equipment is utilized in a commercial environment, the rules of FCC Part 15-J, Class A apply. Connection and operation of this equipment with other equipment that is verified to comply with the Rules applicable to Class A (Commercial) use is typically acceptable in the commercial use environment. Refer to the instructions supplied with the FCC Class A systems intended for interconnection to this equipment for direction.

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna.
- Relocate the computer with respect to the receiver.
- Move the computer away from the receiver.
- Plug in the computer to a different outlet so that computer and receiver are on different branch circuits.

If necessary, consult the dealer or an experienced radio/television technician for additional suggestions.

Preface

The AT&T UNIX® PC Reference Manual has been written for technicians doing component-level troubleshooting of the AT&T UNIX® PC logic board.

Organization of this Manual

This manual contains the following sections:

System Features and Functions

Briefly describes the physical features and functional capabilities of the UNIX PC system.

Logic Board Theory of Operation

Describes the logic board hardware and the functions performed by it, including direct memory access and bus arbitration, machine cycle timing, memory management, and input/output handling.

Diagnostics

Describes boot ROM, floppy disk, and expert mode diagnostics, including algorithms, screen displays, and error messages.

Logic Board Test Procedures

Contains a collection of test procedures intended to aid in troubleshooting.

Schematics

Contains the schematic of the logic board for P4 and P5 configurations and schematics for DMA and video gate arrays.

Appendix A: PAL Equations

Contains the logic equations for the arbitor, disk interface, memory management unit, and hard disk data separator PALs.

Appendix B: Mnemonics

Contains definitions of the mnemonics used throughout the theory of operation and the schematics.

Appendix C: Expansion Memory Locations

Contains a table listing of the possible expansion memory configurations and their expansion slot position requirements.

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System Features
and Functions

System Features and Functions

1 System Features and Functions

The **UNIX** PC is an intelligent desktop workstation that provides users with personal computing and enhanced voice and data communications services. It provides the UNIX System V virtual memory operating system in a telephone network environment. The **UNIX** PC can connect to a telephone system to allow communication with other telephones, workstations, and computers. Direct connection, or connection through a local area network, to other terminals, workstations, or computers, is also provided. The **UNIX** PC can be upgraded to a multiuser system.

The **UNIX** PC consists of the following parts, as illustrated in Figure 1-1:

- Base unit
- Keyboard
- Mouse

The workstation base unit houses the monitor, power supply, hard disk drive, floppy disk drive, logic board, and three expansion slots. The logic board provides the processor logic, bit-mapped graphics logic, communications, and interface logic for all connected input/output (I/O) devices. The monitor is attached to a base that allows it to tilt and swivel.

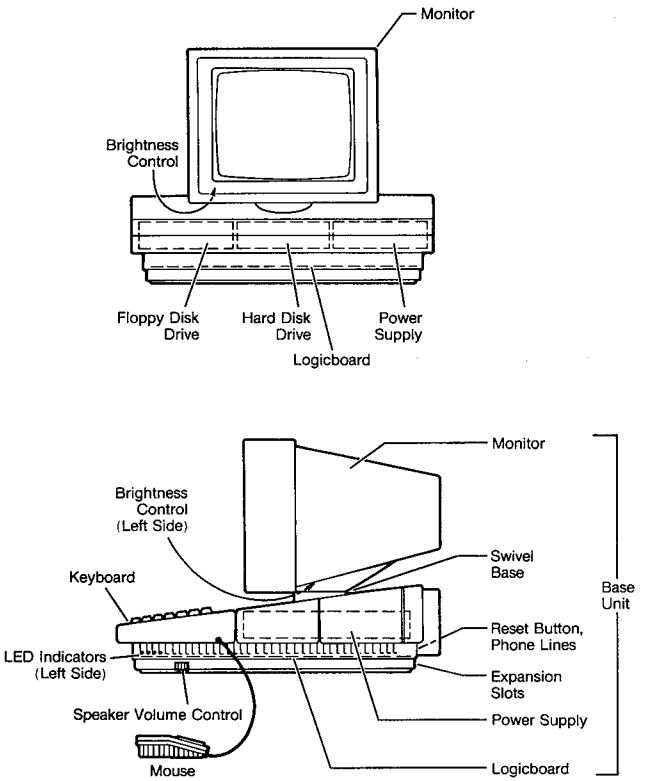


Figure 1-1 Base Unit, Keyboard, and Mouse

Functional Specifications

These specifications describe the major circuitry and general characteristics of the **UNIX** PC system.

Logic Board

The Logic Board is shown in Figure 1-4.

- Motorola 68010 central processing unit (CPU) with 10-megahertz (MHz) clock
- Virtual memory address space of 4 megabytes (MB)
- 0.5MB, 1 MB standard or 2 MB random access memory (RAM)
- 720 by 348 bit-mapped graphics monitor interface
- DTE RS-232-C serial port
- Centronics-compatible parallel printer port
- Keyboard interface
- Telephone interfaces for voice and data service. Three modular jacks are used: one for connection to a user-provided telephone and the other two for connection to tip/ring telephone lines. Also included is an integrated 300/1200 bits per second (bps) modem compatible with AT&T Models 103 and 212, offering asynchronous operation and autobaud capabilities.
- Hard disk interface
- Floppy disk interface
- Expansion bus interface that allows memory and I/O expansion. The bus has 21 address lines and 16 data lines and supports bus mastership by expansion hardware
- A realtime clock that retains the time and date when the **UNIX** PC is powered down

Terminal Subsystem

The monitor contains a 12-inch cathode ray tube (CRT), a deflection board, and a yoke. It provides a 20-MHz screen capable of displaying 720 by 348 pixels. The display can be programmed either as light on dark (normal) or dark on light (inverse video).

The monitor is attached to the base. The monitor tilts -5 to +20 degrees relative to the horizontal plane and swivels.

The screen is treated to reduce glare. A brightness control is accessible to the operator, as shown in Figure 1-1.

Keyboard

The keyboard is shown in Figure 1-2.

The keyboard is connected to the base with a flexible, coiled cord that can expand to approximately six feet. One end of the cord has about an inch of straight cord that plugs into the base unit. Both ends of the cable have connectors that prevent accidental disconnection.

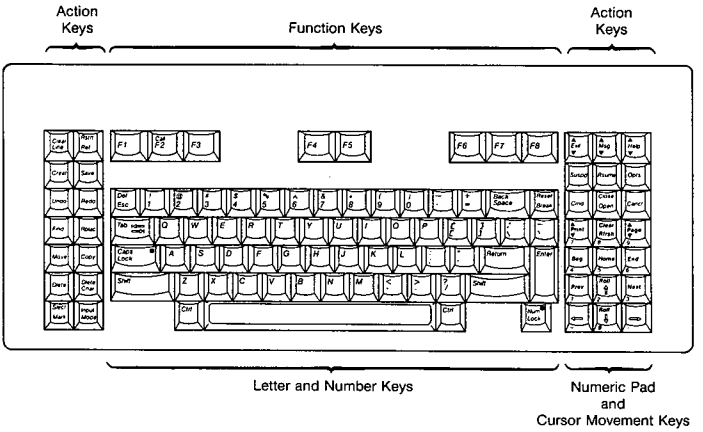


Figure 1-2 Keyboard Layout

Mouse

The mouse connects to the keyboard unit with a lightweight, uncoiled cord that is approximately four feet long. The cable has a connector that locks preventing accidental disconnection. The cord plugs into the keyboard. These connections are shown in Figure 1-3.

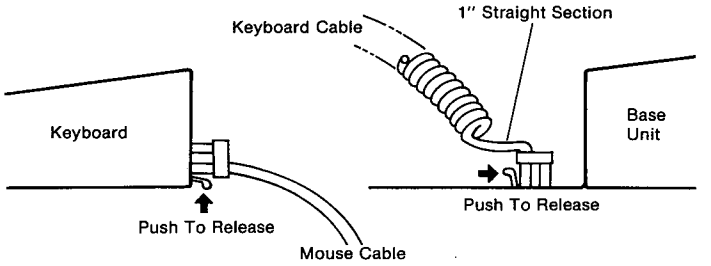


Figure 1-3 Keyboard and Mouse Connections

Audible Indicator

An audible indicator consisting of a small speaker is provided for monitoring telephone calls when using the AT&T **UNIX** PC Telephone Manager. A user-accessible slide volume control, illustrated in Figure 1-1, is located just under the right edge of the base unit.

Data Storage

Data can be stored either on a hard disk which is part of the **UNIX** PC system, or on floppy disks using the floppy disk drive. The storage capacities available are:

- A 10MB, 20MB, 40MB or 67MB hard disk (Winchester) for mass storage
- A double-sided, 1/2-MB (320 Kb formatted), 5 1/4-inch, 48-tpi floppy disk drive

RS-232-C Port

The RS-232-C port supports both synchronous and asynchronous data communications. Asynchronous bit rates of 110 bps to 19.2 Kbps are available.

RS-232-C Signals

The following table of signals applies to the RS-232-C connector. The table gives the pin number, signal name, and direction for the **UNIX** PC.

Table 1-1 RS-232-C Signals

Pin	Name	Direction
1	Ground (shield)	-
2	Transmit data	Output
3	Receive data	Input
4	Request to send	Output
5	Clear to send	Input
6	Data set ready	Input
7	Ground (signal)	-
8	Carrier detect	Input
15	Transmit clock	Input
17	Receive clock	Input
20	Data terminal ready	Output
22	Ring indicator	Input
24	DTE transmit clock	Output

Channel B of the 8274/7201 multiple protocol serial controller is connected to the modem. The following list describes the channel B signals:

8274/7201 Carrier detect <---RS-232-C ring indicator

8274/7201 Receive clock <----Modem receive clock

8274/7201 Clear to send <----RS-232-C data set ready

8274/7201 Transmit data----> Modem transmit data

8274/7201 Transmit clock <---Modem transmit clock

8274/7201 Receive data <-----Modem receive data

RS-232-C Signal Levels

Figure 1-4 illustrates the possible RS-232-C cabling to a printer or terminal.

Signal levels are +/-12V nominal.

UNIX PC to Terminal Cable Pinning

UNIX PC		Terminal
1	----------	1
2	---------->	3
3	<----------	2
4-5-6		4-5-6
7	----------	7
8	---------->	20
20	<----------	8

UNIX PC to Printer with CTS Control

UNIX PC		Printer
1	----------	1
2	---------->	3
3	<----------	2
4	<---------->	4
6-8-20		
5	----------	7

Figure 1-4 RS-232-C Cabling

Diagnostic Loopback Plug

The diagnostic floppy tests RS-232-C functions through the use of a loopback plug, which must be installed when a channel is being tested.

Loopback plug (male) pinning is shown in Figure 1-5.

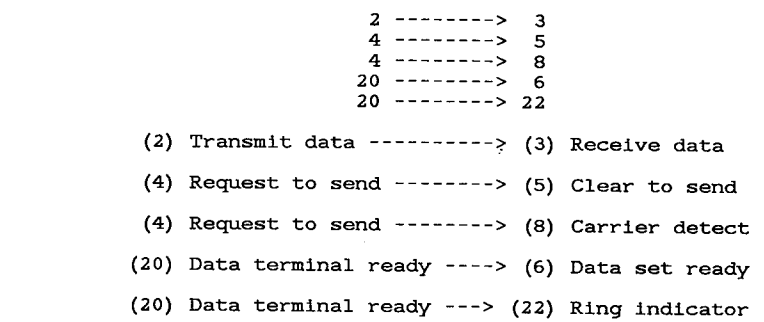


Figure 1-5 Loopback Plug Pinning

Centronics Parallel Printer Interface

Table 1-2 is an example of how a parallel printer cable might be constructed for a Centronics printer. The **UNIX** PC has an Amphenol 57 series 36-pin connector. This is a standard Centronics connector.

Cable Pinning

The following guidelines showing the printer signal requirements do not have to be adhered to strictly when building your own cable (in the case of signal ground). Signal ground is tied to pins 16, 17, 19-30, 33, and 36 on the **UNIX** PC connector.

Make sure your printer is strapped for negative strobes and acknowledges. Do not let any signals float. For example, if you are not going to use BUSY+, ground it.

This table shows typical pin functions for the Centronics printer cable:

Table 1-2 The Parallel Interface

Signal Pin	Return Pin	Signal	Direction	Description
1	19	$\overline{\text{STROBE}}$	OUT	Pulse to read data in. Pulse width should be 0.5 ms at the receiving terminal.
2	20	DATA 1	OUT	These signals represent information of the 1st to 8th bits of parallel data, respectively. Each signal is at HIGH level when data is logical 1 and LOW when it is logical 0.
3	21	DATA 2	OUT	
4	22	DATA 3	OUT	
5	23	DATA 4	OUT	
6	24	DATA 5	OUT	
7	25	DATA 6	OUT	
8	26	DATA 7	OUT	
9	27	DATA 8	OUT	
10	28	$\overline{\text{ACKNLG}}$	IN	Approximately 12-microsecond pulse. LOW indicates that data has been received and that the printer is ready to accept more data.
11	29	BUSY	IN	A HIGH signal indicates that the printer cannot receive data. The signal goes HIGH in the following cases: o During data entry o During printing o When offline o During printer -error state
12	30	PE	IN	A HIGH signal indicates that the printer is out of paper.

Table 1-2 The Parallel Interface (Continued)

Signal Pin	Return Pin	Signal	Direction	Description
13	--	LP SELECT	IN	Pulled up to +5 volts through a 1K-ohm resistor.
14	--	$\overline{\text{AUTO FEED XT}}$	OUT	This signal is pulled up to +5 volts through a 1K-ohm resistor.
15	--	NC	--	Unused.
16	--	OV	--	Logic ground level.
17	--	CHASSIS GND	--	Printer's chassis ground, which is isolated from the logic ground.
18	--	NC	--	Unused.
19-30	--	GND	--	Twisted-pair return signal ground level.
31	--	$\overline{\text{INIT}}$	OUT	This signal is pulled up to +5 volts through a 1K-ohm resistor.
32	--	$\overline{\text{ERROR}}$	IN	This level becomes LOW when the printer is in: o Paper-end state o Offline o Error state.
33	--	GND	--	Same as for pins 19-30.
34	--	NC	--	Unused.
35	--	NC	--	Unused.
36	--	$\overline{\text{SLCT IN}}$	OUT	Signal ground level.

Notes

- The column heading "Return" denotes the twisted-pair return, to be connected at signal ground level. For the interface wiring, be sure to use a twisted-pair cable for each signal and to complete the connection on the return side. To prevent noise, these cables should be shielded and connected to the chassis of the host computer and the printer, respectively.
- The column heading "Direction" refers to the direction of signal flow as viewed from the base unit.
- All interface conditions are based on TTL level. The rise and fall times of each signal must be less than 0.2 microseconds.

Status Signal Description

- LPNOPAPER+: Centronics pin 12, asserted by printer when paper-out sensor senses no paper in the printer.
- LPBUSY+: Pin 11, asserted by the printer to indicate that it cannot receive data. Also indicates a paper empty or fault condition.
- LPSELECT+: Pin 13, asserted by printer to indicate that it is selected and ready to receive data.
- ERROR*: Pin 32 asserted when there is a problem with the printer.
- LPACK*: Pin 10, asserted by line printer to indicate that it has received data.

Expansion Slots

Three expansion slots are provided as part of the base unit. Expansion cards can be installed in any slot. However, depending on the memory being added, they must be located in accordance with the expansion memory location matrix in Appendix C.

Expansion slots support expansion boards including those listed below:

- 0.5MB or 2MB expansion RAM board
- Three versions of combo boards

  0.5MB, 1MB or 1.5MB with two RS-232 ports
- MS-DOS expansion board
- Two port RS-232 only board
- Interface board for tape backup (floppy tape)
- Interface board for tape backup (QIC-02)

Expansion boards may dissipate up to 12 watts each.

Physical and Electrical Specifications

The basic characteristics of the **UNIX** PC are:

- Base unit: Approximately 18 inches wide, 17 inches deep, and 16 inches high; weighs approximately 40 pounds.
- Keyboard: AT&T 103-key, low-profile design.
- Electrical: 100-130 volts; maximum power under 400 watts.

Logic Board Bus System

This section describes the logic board bus system, including the address and data bus and the system control block diagram, which explains how bus transfers are regulated. Figure 1-6 shows the layout of the **UNIX** PC logic board.

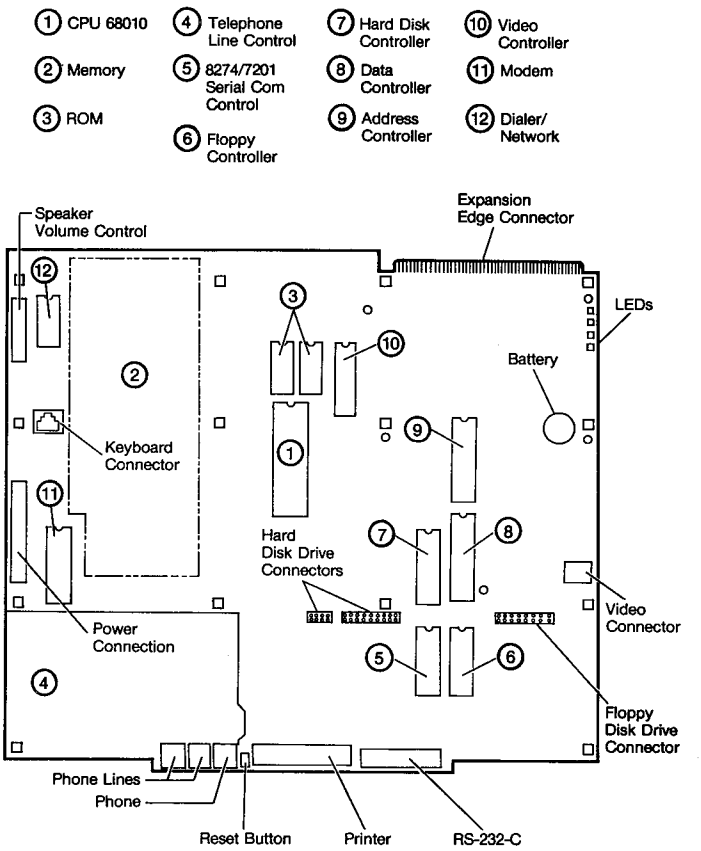


Figure 1-6 Logic board

Simplified Address and Data Block Diagram

The system block diagram in Figure 1-7 shows how the system bus allows the various devices within the **UNIX** PC CPU board to transmit data to each other.

The right half of the drawing shows the peripheral devices. Each peripheral has special control interface circuitry that modifies information coming from or going to the peripheral into a form that is acceptable for the bus and the peripheral. These circuits are indicated in the drawing by the rectangular boxes marked **bit map, printer port, telephony controller,** and so on. The bus accepts data 16 bits wide. The keyboard, for example, generates data in the form of a serial bit stream. These control interface circuits also receive control signals that initiate and terminate data transfers.

The left half of Figure 1-5 shows devices that do internal information processing. These include the 68010 CPU and the three forms of memory: ROM, RAM, and disk storage. The bus itself is really two buses, a data bus and an address bus.

The data bus consists of 16 bits, labeled D0-D15, for transmission of 16-bit data words. The address bus consists of 23 bits, labeled A1-A23. (There is an A0 function that is internal to 68010.)

Data transfers on the **UNIX** PC bus are performed using a master-slave system. A master device such as the 68010 begins a transfer by first putting an address on the address bus to identify the device with which it will perform a data transfer. Then, depending on the direction of the data transfer, either master-to-slave or slave-to-master data is loaded onto the data bus, and the transfer takes place.

In the **UNIX** PC, the 68010 and the DMA (direct memory access) controller are both masters. There are other possible masters that are not shown for simplicity. Any of the devices on the right side of the drawing can be slaves to the 68010. The DMA controller for the disk drives transfers data only to RAM memory, so it has only one slave.

Before starting a DMA transfer, the 68010 must load information into the DMA controller, in which case the DMA controller is acting as a slave to the 68010. During the transfer, the DMA controller generates appropriate control signals that cause the transfer to begin and end and also determine the direction of the transfer, either from master to slave or slave to master. On the drawing, arrows indicate the direction of transfer. Notice that the address bus differs from the data bus in that the address bus allows only a one-way transfer of information, from master to slave. The data bus allows two-way transmission, as indicated by the arrows.

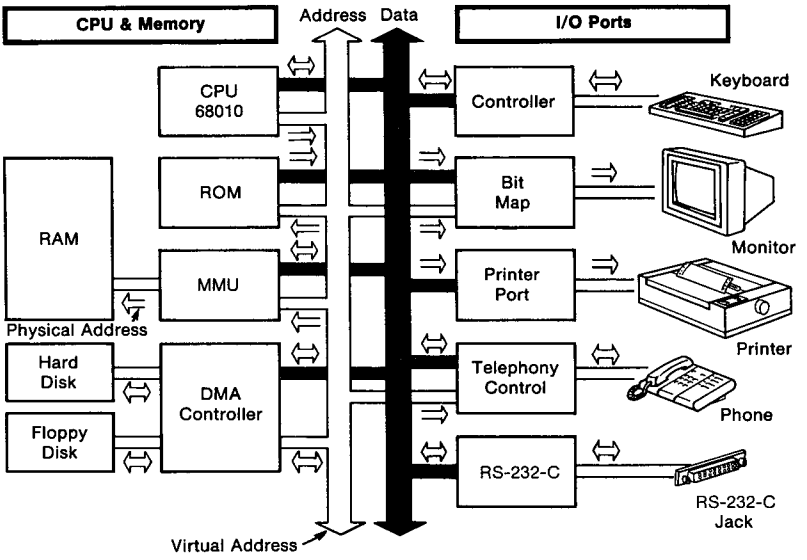


Figure 1-7 Bus System Block Diagram

Onboard Memory

Memory in the UNIX PC consists of both Random Access and Read Only memory, both are located on the logic board.

Random Access Memory

The logic board provides a minimum of 512 KB of onboard RAM, which can be expanded to either 1 or 2 MB maximum. A minimum memory configuration is made up of 72 type 4864, 64K by 1-bit dynamic RAM chips. The **1MB logic board** is made up of 36 type 4256, 256K by 1 bit, dynamic RAM chips. The **2MB logic board** is made up of 72 type 4256, 256K by 1 bit, dynamic RAM chips.

The memory is used for program execution. It is organized into a virtual memory system, which allows the programmer to write programs as if there were a much larger amount of memory available than is physically present. The **UNIX** PC virtual memory system is 4 MB. The hardware provides this function through a special set of memory chips called page map RAMs. These RAMs are 1K by 4-bit static RAM chips.

Read Only Memory

The logic board contains two 2764 8-KB or two 27128 16-KB ROM chips. They hold the initialization program that is run when the power is turned on or the Reset button is pressed, or a software reboot command is exercised.

System Control Block Diagram

The system control block diagram, Figure 1-8, shows how the system determines which bus master controls the bus at any given time. There are three elements to system control: interrupt, memory management, and bus arbitration.

The right side of the drawing shows the I/O controller logic. When a peripheral device such as the keyboard wants to send data to the system, its controller sends an interrupt signal to the interrupt logic. This is one method of communication between an I/O device and the system.

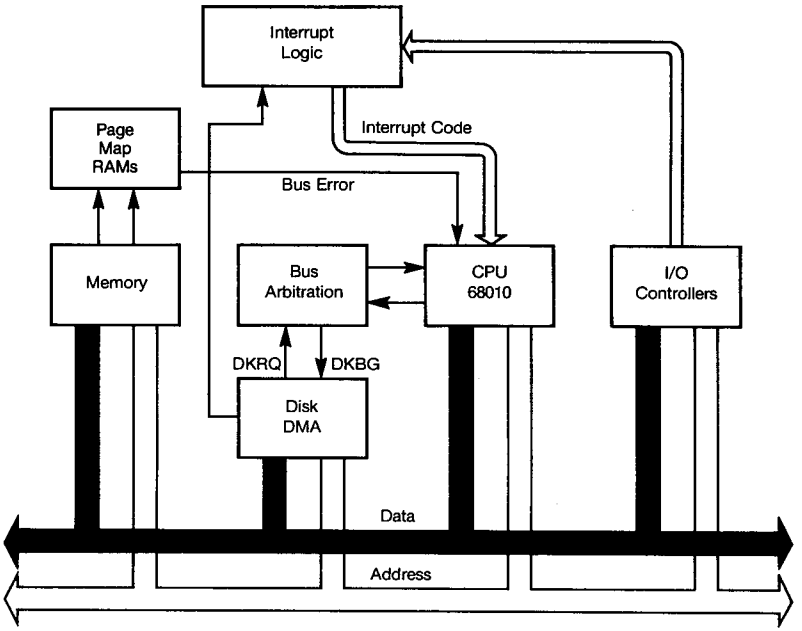


Figure 1-8 System Control Block Diagram

The interrupt signal is compared to a priority list. The highest priority pending at any given time causes the interrupt logic to send a signal to the 68010. The 68010 then responds by performing a sequence of data movements called an interrupt processing sequence. The function of the interrupt acknowledge is to allow the processor to store its current status so it can return to the same state after responding to the interrupt.

First it completes execution of its current instruction and stores the status of its internal registers. Then it jumps to an interrupt service program that determines which device generated the interrupt. Finally, it jumps to a program to service that particular interrupt. Interrupt priorities are listed in Table 1-3.

Table 1-3 Interrupt Priorities

Priority Level	Device
7 (highest)	Parity error or MMU error (logic board)
6	60-Hz (logic board)
5	Expansion slots 1, 2, and 3
4	274/7201 communication (detection circuit, RS-232-C)
3	Keyboard/mouse, modem
2	Hard disk drive, floppy disk drive, or line printer
1 (lowest)	Expansion slots 1, 2, and 3

Note: Levels 1 and 5 are available to expansion slots 1, 2, and 3.

Memory Management

A second element of system control is the memory management unit shown on the left in Figure 1-6. This unit monitors every access to the dynamic RAM memory chips. Certain accesses cause a memory management error. For example, if a user program attempts to write to a memory address that has been defined as being in disk address space and not in physical RAM, the memory management unit generates a signal called a bus error.

Bus Arbitration

At some point two bus masters will both want control of the bus. The third element of system control, the bus arbitration unit, resolves the conflict. It evaluates requests for bus control from masters and grants bus control on a priority basis. The 68010 has lower priority than the disk controller. The 68010 has to wait for the disk controller to release control of the bus before it can take control.

Table 1-4 Bus Arbitration Priorities

Priority Level	Device
6 (highest)	Refresh
5	Expansion slot 1
4	Disk Interface Hard and Floppy
3	Expansion Slot 2
2	Expansion Slot 3
1 (lowest)	68010 CPU

Data Storage Device Specifications

The following tables list specifications for both types of storage device used on the UNIX PC system. These tables are arranged by manufacturer for each drive offered on the Model 7300 and 3B1 machines.

Table 1-5 Hard Disk Drive

Manufacturer	Specifications		
Miniscribe	Capacity Unformatted	Per Drive	12.0 MBytes 25.0 MBytes 53.0 MBytes 85.0 MBytes
		Per Track	10,416 Bytes
	Formatted	Per Drive	10.0 MBytes 20.0 MBytes 44.0 MBytes 67.0 MBytes
		Per Track	8,192 Bytes
		Per Sector	512 Bytes
		Sectors per Track	16

Table 1-5 Hard Disk Drive (Continued)

Manufacturer	Specifications	
Miniscribe (cont.)	Functional	Rotational Speed (RPM) 3600 Recording Density (bpi) 10,030 for 10, 20MByte Drives 9,950 for 40, 67MByte Drives Area Density (M/bit/sq/in) 5.9 Track Density (tpi) 588 for 10, 20MByte Drives 1000 for 40, 67MByte Drives Total Data Tracks 2,448 Cylinders 612 for 10, 20MByte Drives 1024 for 40, 67MByte Drives R/W Heads 10MByte 2, 20MByte 4, 40MByte 5, 67MByte 8
	Data Transfer Rate	(Mbits per second) 5.0
	Access Time (includes settling)	**10 and 20MByte** Average (msec) 85 Track-to-Track (msec) 15 Maximum (msec) 190 Latency (average, msec) 190 **40 and 67MByte** Average (msec) 30 Track-to-Track (msec) 3 Maximum (msec) 60 Latency (average, msec) 60
	Interface	ST412
	Error Rates Soft Read Errors 1 per 10^{10} bits transferred Hard Read Errors 1 per 10^{12} bits transferred Seek Errors per 10^{6} seeks	

Table 1-5 Hard Disk Drive (Continued)

Manufacturer	Specifications
Miniscribe (cont.)	DC Power Requirements **10MByte** +5V DC +/- 5%, 0.75 amps +12V DC +/-5%, 0.75 amps **20MByte** +5V DC +/- 5%, 0.4 amps +12V DC +/-5%, 1.0 amps **44MByte** +5V DC +/- 5%, 0.6 amps +12V DC +/-5%, 1.0 amps **67MByte** +5V DC +/- 5%, 0.6 amps +12V DC +/-5%, 2.0 amps
	Max Starting (10 sec) 3.5 amps
	Power Dissipation 14 watts

Table 1-5 Hard Disk Drive (Continued)

Manufacturer	Specifications	
Hitachi	Capacity Unformatted	Per Drive 51.0 MBytes Per Track 10,416 Bytes
	Formatted	Per Drive 40.0 MBytes Per Track 8,192 Bytes Per Sector 512 Bytes Sectors per Track 16
	Functional	Rotational Speed (RPM) 3600 Recording Density (bpi) 9,340 Area Density (M/bit/sq/in) 5.9 Track Density (tpi) 784 Total Data Tracks 2,448 Cylinders 714 R/W Heads 7 Disks 2
	Data Transfer Rate	(Mbits per second) 5.0
	Access Time (includes settling)	Average (msec) 30 Track-to-Track (msec) 8 Maximum (msec) 55
	Interface	ST412
	Error Rates Soft Read Errors 1 per 10^{10} bits transferred Hard Read Errors 1 per 10^{12} bits transferred Seek Errors per 10^{6} seeks	
	DC Power Requirements +5V DC +/- 5%, 0.4 amps typical +12V DC +/-5%, 1.0 amps typical Max Starting (10 sec) 3.5 amps	
	Power Dissipation	14 watts

Table 1-6 Floppy Disk Drive (Winchester)

Manufacturer	Specifications	
Teac	Capacity Unformatted	Per Disk Single Density 250KBytes Per Disk Double Density 500KBytes Per Track 3,125KBytes Single Density, 6.25KBytes Double Density
	Formatted	Per Disk Single Density 163.84KBytes Per Disk Double Density 327.68KBytes Per Track Single Density 2,048KBytes Per Track Double Density 4,096KBytes Per Sector Single Density 256 Bytes Per Sector Double Density 512 Bytes Sectors per Track 8
	Functional	Rotational Speed (RPM) 300 Recording Density (bpi) Single Density 2,938 Double Density 5,876 Area Density (M/bit/sq/in) 5.9 Track Density (tpi) 48 Total Data Tracks 80

Logic Board Theory of Operation

Logic Board
Theory of Operation

2 Logic Board Theory of Operation

This overview summarizes the major functions performed by the logic board hardware. In addition, it describes the boot ROM program algorithm.

The logic board hardware functions include:

- Direct memory access and bus arbitration
- Machine cycle timing
- Memory management
- Input/output handling

Direct Memory Access

The **UNIX** PC bus is shared by the 68010 central processing unit (CPU) and several direct memory access (DMA) devices, such as the disk bus interface unit, dynamic RAM refresh, and expansion boards. During a DMA transfer, the 68010 waits while data is moved directly from a DMA device, such as the disk bus interface unit, into RAM memory. DMA provides high-speed transfer of blocks of data to or from memory.

Machine Cycle Timing

A 68010 machine cycle consists of putting an address on the bus, transferring data, and releasing the bus. Machine cycles are either fast (400 nanoseconds) or slow (1100 ns). Access to the lower half of the address space results in a fast cycle; access to the upper address space results in a slow cycle. DMA machine cycles are considered fast (500 ns). The additional 100 ns is needed in this case to do bus arbitration.

Memory Management

Programs run on the UNIX PC are often too large to fit in the RAM memory chips on the logic board. Thus, when the system is booted up, only a portion of the program is loaded into memory. While the program is being executed, it is monitored by memory management hardware. When a portion of the program that is on the disk is needed, the memory management hardware generates an error, causing the DMA to move the required portion of the program from the disk drive into RAM memory.

The processor can address locations anywhere in the entire 16 megabytes (MB) of system space, but the DMA can access only the lower 1/4 of system address space that is used by RAM (physical memory space).

Input/Output Handling

Input and output (I/O) operations are memory mapped--that is, the 68010 does not have separate instructions for I/O operations. I/O ports are accessed by assigning addresses to them. I/O operations are handled either by interrupt or by polling. Polling is used in boot ROM programs where stack operations are forbidden. Table 2-1 lists the 68010 processor pin functions.

Boot ROM Algorithm

The boot ROM is used for program memory following power up, hard reset (reset switch), or a software generated re-boot. The boot ROM program tests memory. Then it initializes the logic board by initializing the status of the memory management hardware and various peripheral controller chips. Then it causes a program to be loaded from floppy or hard disk and jumps to that program.

Table 2-1 68010 Processor Pin Functions

Pin No.	Mnemonic	Description
29-52	A1-A23	23-bit address bus (outputs only)--A unidirectional, three-state bus capable of addressing 16 MB of data. Provides addressing for all CPU cycles except space cycles.
1-5 54-64	D0-D15	16-bit data bus--Bidirectional, three-state bus that is the general-purpose data path. Transfers either words or bytes.
6	AS	Address strobe--Signal indicating there is a valid address on address bus.
7-8	UDS, LDS	Upper and lower data strobes--Signals used with R/W to control data flow on the data bus. UDS enables the upper byte; LDS enables the lower byte. When both are active, words are transferred.
8	R/W	Read/Write Defines the data bus transfer as a read or write cycle.
10	$\overline{\text{DTACK}}$	Data transfer acknowledge--Input indicating that a data transfer has been completed. When received during a read cycle, data is latched one clock cycle later and the bus cycle is terminated. When received during a write cycle, the bus cycle is terminated.
13	$\overline{\text{BR}}$	Bus request--Not used
11	$\overline{\text{BG}}$	Bus grant--Not used
12	$\overline{\text{BGACK}}$	Bus grant acknowledge--Not used

Table 2-1 68010 Processor Pin Functions (Continued)

Pin No.	Mnemonic	Description
23-25	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	Interrupt priority level 0-2--Inputs indicating the encoded priority level of the device requesting to interrupt the CPU. Level 7 has highest priority, and level 0 indicates no interrupts present. Level 7 cannot be masked. These inputs must remain stable until the processor acknowledges, which is accomplished by setting FC0-FC2 and A04-A23 high.
26-28	FC0,FC1,FC2	Function code 0-2--Outputs activated along with address strobe to indicate the state (user or supervisor) and the cycle type currently being executed. FC2 FC1 FC0 Cycle Type Low Low Low (Undefined) Low Low High User data Low High Low User program Low High High (Undefined) High Low Low (Undefined) High Low High Supervisor data High High Low Supervisor program High High High CPU space
15	CLK	Clock--10-MHz input, internally buffered for development of timing needed internally by the processor.
20	E	Enable--Not used
19	VMA	Valid memory address--Not used
21	$\overline{VPA}$	Valid peripheral address--Asserted during an interrupt cycle to inform the CPU that the current interrupt cycle is an autovector cycle. As implemented in the **UNIX** PC, all interrupts are autovectored.

Table 2-1 68010 Processor Pin Functions (Continued)

Pin No.	Mnemonic	Description
22	$\overline{\text{BERR}}$	Bus error--Input informing the CPU that there is a problem with the current cycle. Most commonly used when applied memory address is not in primary memory.
17	$\overline{\text{HALT}}$	Halt--Bidirectional. When used as input, the processor floats all outputs and stops at the completion of the current bus cycle. Other uses are described below.
18	$\overline{\text{RESET}}$	Reset--Bidirectional signal that resets the system upon power up or pressing the Reset button. The reset and halt inputs are tied together to ensure a total processor reset. Pressing the Reset button for 10 clock cycles causes a total system reset. Upon power up, reset and halt must be driven low for at least 100 ms. A software reset causes the reset signal to be driven for 124 clock cycles.

Note

An alphabetical listing of mnemonics used in this section appears in Appendix B.

Fast and Slow Cycles

68010 machine cycles are either fast (400 ns) or slow (1100 ns) depending on the address being accessed. The slow cycle is achieved by delaying the arrival of data transfer acknowledge (DTACK) to the 68010. A custom IC containing the timing circuit determines how much delay to provide through address decoding. DMA machine cycles are fast (500 ns) transfers between the DMA devices and RAM memory or refresh of RAM memory.

Table 2-2 shows how the two most significant address bits are decoded to select fast or slow cycles:

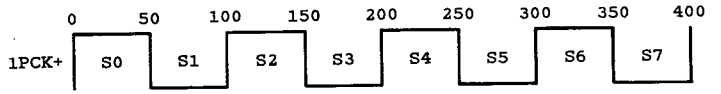
Table 2-2 Significant Address Decoding

A23	A22	Region Description
0	0	RAM memory: fast-cycle access by 68010 user or supervisor mode
0	1	I/O registers: fast-cycle 68010 access in supervisor mode only
1	0	ROM memory: slow-cycle 68010 read in supervisor mode only
1	1	I/O registers: slow-cycle 68010 access in supervisor mode only

From the program execution viewpoint, fast and slow cycle transfers are identical. An instruction is executed in the same way except that the CPU waits longer for an acknowledge signal during slow-cycle transfers.

The CPU adjusts the length of its machine cycle to meet the requirements of the bus. It drives address and control signals and waits for DTACK data transfer acknowledge (pin 10).

The 68010 is clocked by a 10-MHz signal called 1PCK. 1PCK is a 50% duty cycle clock with a full-cycle duration of 100 ns. The CPU uses four PCK cycles to accomplish a fast bus cycle. These four cycles are used as eight states (S0-S7) by the 68010:



The CPU samples DTACK* at the trailing edge of S4. If DTACK* is present at the trailing edge of S4, the CPU latches data (for a read), tristates control signals at the trailing edge of S6, and tristates its address lines at the trailing edge of S7.

If DTACK* is not present, the processor begins inserting wait states and sampling DTACK* at the trailing edge of each succeeding 1PCLK. When DTACK* arrives, the processor behaves as described in the preceding paragraph.

For a slow processor cycle, the hardware simply prevents the generation of DTACK* for an extra six clock cycles. The extra time is allotted for the slow response of the ROM and I/O devices. This describes the difference between a fast cycle and a slow cycle.

68010 CPU machine cycles are either instruction fetches or instruction execution cycles. The 68010 outputs status bits that identify the type of cycle being performed. These status bits can be used by a logic analyzer to display only program execution to aid in troubleshooting.

Clock Generation

Sheet 3 refers to schematic sheet 3. Note that integrated circuits (IC) are referred to by their location identifiers. For example, 21F refers to an IC located at position 21F on the logic board. As seen from the front of the UNIX PC, parts on the logic board are identified with two coordinates, numbers from left to right (1-28) and letters from front to back (A-P).

System clock signals are generated as follows:

- A 40-MHz oscillator provides the source frequency for the majority of the system clocks.
- This frequency passes through OR gate 21F and provides the clock for dual J-K F/F 20G.
- Pins 9 and 7 of 20G output a 20-MHz signal, and pins 5 and 6 output 10 MHz.
- These signals are buffered by 19G and output as 20MCK, X20MCK+, XPCK+, PCK*, 1PCK+ 2PCK+.
- 1PCK+ feeds the clock input of F/F 16K and causes the generation of the 5-MHz signal, 5MCK+.
- 1PCK+ feeds the DMA address IC (22E, sheet 9) and causes the generation of the 1-MHz signal, 1MCK+.

Bus Arbitration

A bus arbitration programmable array logic (PAL) decides which DMA device is granted accesses to the bus when two DMA devices request the bus at the same time. When no DMA devices are requesting the bus, the 68010 controls the bus.

Bus Masters and Slaves

The **UNIX** PC uses a system address and data bus as shown in Figure 2-1. The system bus makes it possible for bus arbitration to switch the bus between several devices, called bus masters.

The devices connected to the system bus are classified as either bus masters or bus slaves. In every data transfer, one device is the master and one is the slave. The master outputs the control signal that starts the transfer and provides the address of the device to or from which it wants to transfer data . A bus slave is connected to the bus when an address decoder detects the presence of the address assigned to that device on the address bus.

Figure 2-1 shows two bus masters in the **UNIX** PC system, the 68010 CPU and the disk DMA controller, and a single device to which they can both transfer data, the RAM memory array.

When the 68010 CPU transfers data to RAM memory, control signals are asserted that enable the tristate buffers and connect the 68010 address and data lines to the system address and data bus. At the same time, other control signals put the DMA circuits inside the custom DMA address and put data and gate array chips in a tristate condition, thus disconnecting them from the system address and data bus.

When the DMA ICs are transferring data between a disk drive and memory, the DMA address counter and data latch are enabled. The 68010 address and data buffers are in a tristate condition.

Diagnostics and Test Procedures

Diagnostics and Test Procedures

3 Diagnostics

There are two types of diagnostics: ROM diagnostics that consist of a program that is an integral part of the hardware, and a floppy disk program contained on a single floppy disk.

Boot ROM Program

The primary function of the boot ROM program is to boot a program that loads the operating system from the hard disk drive or the diagnostics from the floppy disk drive. In addition, the boot ROM includes a number of diagnostic tests. It tests ROM, RAM memory, and video memory; it also programs the initial status of the memory management hardware and various peripheral controller chips.

During execution, the boot ROM program turns a set of LEDs on and off in appropriate binary number patterns as it completes its tests. The LEDs are visible through the ventilation slots on the left side of the system. (The ROM test executes so fast that the blinking on and off of the LEDs is not be noticed.) The successful completion of each test starts the next. If a test fails, the binary number pattern of that test continues to be displayed as long as the power is on.

Pressing the Reset button or turning on the power causes the boot ROM diagnostics program to execute.

The following descriptions of boot ROM program steps include address and data information for setting up a logic analyzer to trace program execution.

Bootstrap Jump

When the Reset button is released, the initial value of the stack pointer is loaded from addresses 800000 and 800002. The address of the first executable instruction is loaded into the program counter from reset vector locations 800004 and 800006. Then the program:

- Writes a data word with D15 high to address E40000, which sets IC7K (pin 7) high (ROMLMAP*, sheet 6).
- Turns off the LEDs by writing 0F00 to address 4A0000. (The LEDs are controlled by the miscellaneous control register, shown on sheet 15 of the schematics in Chapter 5.)

Initializing the System

To initialize the system, the program writes 0700 to address 4A0000, which sets the LEDs to binary 1. (Note: Data and address are in hexadecimal notation.)

Initializing the 7201 Serial Port Controller

To initialize channels A and B of the 7201 serial port controller, the program:

- Sets LEDs to 1.
- Resets the error registers by writing 18 to addresses E50004 and E50006.
- Writes F0 to addresses E50004 and E50006.

Initializing the Keyboard

To initialize the keyboard, the program:

- Resets the keyboard controller by writing 0300 to E70000.
- Sets the keyboard controller to eight bits per character with one stop bit by writing 9500 to E70000.

Initializing the Modem

To initialize the modem, the program:

- Disconnects the modem from lines 1 and 2 by writing 8000 to E44000 and E45000.
- Resets the modem by writing 0001 and then 0000 to E60000.

Initializing the Telephone Line Control

To initialize the telephone line control, the program:

- Enables the handset by writing 4000 to 490000
- Selects line 1 by writing 4000 to 491000
- Reads the telephone status register at 450000.

If bit D0 is a 0, the handset is onhook, so the program writes 4000 to 492000 and 496000 to open relay 1 and line 1.

If bit D0 is a 1, the handset is offhook, so the program writes 0 to 494000 and 495000, and then 4000 to 493000 and 497000, to maintain line 1.

Clearing the Printer Interrupt

To clear the printer interrupt, the program writes 0000 to 4F0000.

Clearing the Dialer Chip

To clear the dialer chip, the program writes 0 to 4B0400 and 4B0800.

Resetting the Disk DMA

To reset the disk DMA, the program writes 0000 to 460000 and 4D0000.

Testing Video RAM

To test video RAM, the program:

- Sets LEDs to 2
- Writes 0000 to 420000, the lowest video address
- Reads the same address (420000)

If the contents are not the same, the program jumps to an error loop. If the contents are the same, the program writes 0001 to address 420002 and continues to read and test.

- Continues incrementing address and data until the last video memory address (427FFF) has been tested.
- Reads back each address and checks to see that the contents are correct.

After each address is read, it is written again in case writing to it will affect the contents of the next address.

- Writes 0000 to all video addresses to clear the screen.

Testing Map RAM Memory

To test map RAM memory, the program:

- Sets LEDs to 3
- Performs the same tests on map RAM memory that were performed on video memory from addresses 400000 through 4007FF
- Sets the unity map by writing to all map RAMs, starting with 400000 and ending with 4007FF
- Writes A000 to address 400000 to map page 0

This sets page status bits D15, D14, and D13 = to 101, which corresponds to page status of page present, write enabled, not yet written to, and unity-mapped.

- Increments the address and data and writes to pages 1, 2, 3, and so on until all pages have been declared present, write enabled, not written to, and unity mapped.

Testing RAM

To test RAM, the program:

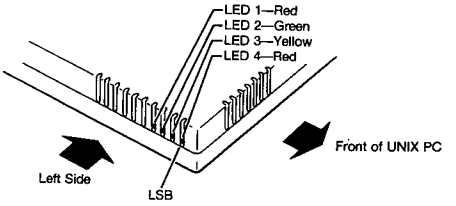
- Sets LEDs to 4.
- Performs the same memory test as before from addresses 000000 through 7FFFFF
- Sets LEDs to 5
- Sets LEDs to 6
- Puts a small inverse video block on the upper-left corner of the screen
- Searches for a loader program

The floppy disk is searched first. If no loader is found or if an error is found, the hard disk is searched. If the hard disk has no loader or has an error (for example, not ready), an inverse video block is added to the screen, and the process is repeated until a loader is found.

Jumping to the Loader Program

When the program finds the loader, it advances the LEDs to 7 and the processor jumps to the loader program.

Figure 3-1 shows the LED locations and off/on patterns for each test.



ROM Tests

Test Number	LED Status 4	3	2	1
Test 1	Off	Off	Off	On
Test 2	Off	Off	On	Off
Test 3	Off	Off	On	On
Test 4	Off	On	Off	Off
Test 5	Off	On	Off	On
Test 6	Off	On	On	Off
Test 7	Off	On	On	On

Figure 3-1 LED Locations and Off/On Patterns

Listed below is the status of the logic board for each LED test number:

Test 1: Failed telephone initialization
Test 2: Failed video RAM test
Test 3: Failed map RAM test
Test 4: Failed to set map RAM to unity map
Test 5: Failed dynamic RAM test
Test 6: Failed initialization
Test 7: Failed to find loader on disk

Note

Any other failure codes indicate a failure to execute the loader program.

Floppy Disk Diagnostics

The floppy disk diagnostics are in two parts, a Main Menu set which exercises the main components of the system, and a subsystem set.

Main Menu Diagnostics Summary

The following list summarizes how the various diagnostic tests from the **UNIX** PC Diagnostics Main Menu are divided into subtests or sequences. Tests that require operator evaluation are labeled interactive. The others, which run without user intervention, are labeled automatic. The automatic tests report failures with error messages. To abort any test still in process, with the exception of formatting tests, type "shift-break".

Test 1: Full System Test (Interactive)

This test consists of the following subsystem tests:

Note

These tests are from the Subsystem Menu, selection 6 of the Main Menu. They are run in order as listed.

- Test 2: Floppy disk
- Test 1: Hard disk
- Test 5: Memory and parity
- Test 9: Processor
- Test 11: Real Time Clock
- Test 7: Modem

Test 2: Initialize Hard Disk (Interactive)

- Requests type of drive
- Formats

Test 3: Enter Bad Blocks (Automatic)

- Modifies bad block table
- Displays VHB

Test 4: Park Disk Heads (Interactive)

- Parks disk

Test 5: Remote Diagnostics (Interactive)

- Allows diagnostics to be run from a remote site

Test 6: Goto Subsystem Menu

- These are a series of tests for subsystem checks

Selection 7: Reboot System

- Reboots the system

Diagnostic Subtest Summary

The following list summarizes the diagnostic tests from selection 6 of the Main Menu. These tests are also divided into subtests or sequences. Tests that require operator evaluation are labeled interactive. The others, which run without user intervention, are labeled automatic. The automatic tests report failures with error messages.

Test 1: Hard Disk (Automatic)

- Recalibration of hard disk
- Random seek of hard disk

Test 2: Floppy Disk (Interactive)

- Formats the floppy disk
- Random seek of floppy disk

Test 3: Keyboard (Interactive)

- Determines whether the keyboard and mouse work properly

Test 4: Video (Interactive)

- Tests all screen parameters

Test 5: Memory & Parity (Interactive)

- Performs data test
- Performs address test
- Performs random pattern test

Test 6: Communications (RS232 Ports) (Automatic)

- Self-test of the RS232 Expansion Ports
- Transfer test at 300 Baud through 19200 Baud

Test 7: Modem (Automatic)

- Internal loopback sequence test used to check:
  - 1200 or 300 Baud
  - no parity, odd parity or even parity
  - 7-bit or 8-bit characters

Test 8: Dialer (Interactive)

- Tests touch-tone pulses
- Tests rotary-dial pulses

Test 9: Processor (Automatic)

- Map RAM test:
  - Data
  - Address
  - Random pattern
- Parity test:
  - Read/write
  - Execution test
- Map translation test:
  - Subtest 1
  - Subtest 2
- Page fault test
- User I/O interrupt test:
  - Subtest 1
  - Subtest 2
- Clock test
- Page protection test

Test 10: Parallel Printer (Automatic)

- Subtest 1 (status test)
- Subtest 2 (transfer test)

Test 11: Real Time Clock (Interactive)

- Read Write test
- Operation test

Test 12: Return to Main Menu

- Returns you to the Main Menu diagnostics

Diagnostic Test Descriptions

The following descriptions include test algorithms, error messages, and screen displays for the floppy disk diagnostic tests.

Memory Test

This test has three subtests: data, address, and random pattern. The same algorithm is used to test map RAM, dynamic RAM, and video memory.

Memory Subtest: Data Test

This test writes a walking ones pattern to a memory location and then reads it back. It tests all memory locations. If the data read back is incorrect, it reports the address, data written, and data read back in the following error message:

Memory error at Address X; Wrote X; Read Back X

Memory Subtest: Address Test

The address test has the following three-step algorithm for each address tested:

- Writes data to a memory location.
- Reverses one bit in the address and writes different data.

- Checks the first address to see if there is a change. If data changes, the test generates an error message reporting the address line that has changed and the memory bank being tested. For example, it writes AAAA to addresss 000000 and then writes 5555 to address 000001. It then reads the contents of address 000000. If the contents are not still AAAA, address line A0 is bad. The following error message appears:

Memory error: Connection on address line X is bad at Bank X

Memory Subtest: Random Pattern Test

During this test, a random number generator sequence generates a 64KB random pattern of 16-bit words. This pattern is then written to memory, repeating every 64KB. Then the random number generator is invoked again, and the pattern is read back from memory and compared with the function generator output.

Memory Test Error Message

If the two patterns differ, the address data written and data read are displayed in the following error message:

Memory error at Address X; Wrote X; Read Back X

Memory Test Screen Display

```
MEMORY TEST

      DATA TEST
      Memory test will begin at 2F000, end at 7FFFF
      Testing.....................................
      ADDRESS TEST
      Memory test will begin at 2F000, end at 7FFFF
      RANDOM PATTERN TEST
      Memory test will begin at 2F000, end at 7FFFF
EXPANSION MEMORY TEST
```

Note

The preceding message is displayed if expansion memory is not present. If it is present, the preceding memory tests are repeated on expansion memory.

Parity Test

This test forces bad parity on each location and checks for an error during each memory access.

It first writes 8000 to address E40000 to set EE+ high at IC7K (pin 4) high. Next it writes 8000 to address E41000 to set PIE+ high (IC7K, pin 5). Then memory is written to and read to see if an interrupt results. If a parity error does occur, the following message appears:

Unexpected parity error at location X

Then the BP+ at IC7K (pin 6) is set low by writing 0 to address E42000. This causes bad parity to be written during any access to memory. Next, a selected memory location is written. Then that location is read. A level 7 interrupt results during the read. This interrupt causes the current address and data to be stored in bus status registers BS0 at address 430000 and BS1 at 440000 and the error bit status to be stored in the general status register at 410000.

Parity Test Error Messages

If the interrupt does not occur, the following messages appear:

No Parity Interrupt at location X
BSR incorrect after parity error at location X
BSR0 = X, BSR1 = X

Parity Test Screen Display

Parity Test

```
PARITY TEST - READ/WRITE TEST
Memory test will begin at 2F000, end at 7FFFF
     Reached Address 30000
     Reached Address 40000
     Reached Address 50000
     Reached Address 60000
     Reached Address 70000
PARITY TEST - SUBTEST 2 EXECUTION TEST
```

Map Translation Test

This test performs the following steps:

- Initializes all pages to one-to-one correspondence between logical and physical address space.
- Checks status bits of map registers. First it writes page present to all addresses and then reads them all. The status bits should show all pages present and read. Next it writes to every location in memory and checks to see that every page shows that it has been written to.
- Interchanges physical and logical page addresses and verifies that content has been interchanged.

The map translation test checks the status bits and page table entry swapping. The subtests are:

- Read/write memory test (checks access and dirty bits)
- Map test (checks page table entry swapping)

Subtest 1 (read/write memory test) performs the following steps:

- Sets status register of a page to valid (01)
- Reads from a memory location on that page
- Reads the status of the page and verifies that it has changed to read (10)
- Writes to a memory location on that page
- Reads the status of the page and verifies that it has changed to written to (11).

Subtest 2 checks mapping to the correct physical memory location as follows:

- Writes to two locations on different pages.
- Swaps the page table entries for the two pages.
- Reads back the two locations and verifies that the values are swapped.

Map Translation Test Error Messages

Subtest 1 can return the following error messages:

Page access bit not set for page number
Page access bits wrong: page number and page bits are X
Page mapping error
Page dirty bit not set for page number

Map Translation Test Screen Display

MAP TRANSLATION TEST
MAP TRANSLATION SUBTEST 1
MAP TRANSLATION SUBTEST 2

Page Protection Test

The page protection test has the following three parts:

o CPU page fault

During this portion of the test, a page is declared not present and the processor generates bus errors by reading and writing to it.

The following error messages may occur during this test:

No page fault received on write
Map add = X, Map = X, Mem add = X

No page fault received on read
Map add = X, Map = X, Mem add = X

Bus Error when none expected
Map add = X, Map = X, Mem add = X

o Writing to page, not write enabled, by user

This portion of the test sets the processor to user mode and writes to a memory page that is write-disabled. It accesses the first location of every page except those used by diagnostics.

The following error messages may occur during this test:

No Bus Error received on write, after page write being disabled
Map add = X, Map = X, Mem add = X

o Access below 512 KB by user

This portion of the test sets the 68010 to user mode and writes to every location below 512 KB except that contained by diagnostics. It verifies BSR0 for MMU, BSR0 and BSR1 for faulted address, and RAM for write-disabled.

The following error messages may occur during this test:

No Bus error detected, while user accessing below 512k memory
Disabled Ram writing failed at mem loca X

BSR incorrect after Bus error at location X
BSR0 = , BSR1 =

Page Protection Test Screen Display

PAGE PROTECTION TEST

Format Disk Test

This test has the following three parts:

- Reads volume home block (VHB) and bad block table (BBT)

This portion of the test reads the VHB and BBT and calculates a check sum. If the check sum is correct, it saves the VHB and BBT to rewrite them later. If the check sum is incorrect or the VHB is not present, new VHB and BBT are written after formatting is complete. Whether check sum is correct or not, it continues formatting.

- Formats all sectors

This portion of the test formats the disk one track at a time. After each track is formatted, it reads the status register to see if an error has occurred.

If the status register reports an error, the following message appears:

Error during Disk Format: Response = XX

(XX is the hexadecimal contents of the status register.)

After the disk is formatted, the VHB and BBT are written and read back and a check sum is calculated. If the check sum is incorrect, the following message appears:

VHB write failed. Disk needs to be re-initialized

If the BBT check sum is bad, the following message appears:

Bad block table write failed. Disk needs to be re-initialized

Format Disk Test Screen Display

FORMAT DISK
Formatting cylinder xx

Recalibration Test

This test has the following three parts:

- Seeks to track 0
- Reads status register for error

If an error is present, the following message appears:

Can't Recal: Response = XX

- Reads VHB and BBT and calculates the check sum

If the check sum is incorrect, the following error message appears:

Recal Failed

Recalibration Test Screen Display

Recal Disk

Surface Test

This test writes 6DB6DB6D to all byte locations in one track, 16 sectors. While writing this pattern, it checks the status register for errors.

If an error occurs, the test determines the number of the sector that has the error by writing 6DB6DB6D to one sector at a time. After each sector is written, the status register is checked. When the error is found, the BBT is updated with the number of the sector that generated the error.

If no errors are generated while the track is being written, the test reads the contents of all 16 sectors and checks the data for any errors.

If an error is found, it reads the sectors one at time to determine the one containing the error and updates the BBT. If no error is found, it checks the next track.

If all tracks are written without error, the test reads all tracks one at a time and checks for error. If an error occurs, it reads each sector to find the one that contains the error and adds it to the BBT.

Surface Test Error Messages

Can't Write the new VHB: Response = XX
Can't Write the new Bad Block Table: Response = XX
Error on Write: Response = XX, Start Block = XX
Error on Re-Read: Response = XX, Start Block = XX
Re-Read Data Fail: Start Block = XX, Byte = XX,
Received XX, Expected XX
Error on Check-Read: Response = XX, Start Block = XX
Check-Read Data Fail: Response = XX, Start Block = XX
Initiating Check Read for pass XX
Bad Block Table Overflow when adding Sector XX
Bad Block Table: Multiple use of alternate XX

Surface Test Screen Display

```
                Surface test
Volume Name: FLOPPY
Pass 1
Testing blocks xxx...yyy
```

User I/O Interrupt Test

This test tries to create a bus fault by having a user program attempt to access a register outside its space. If this does not cause a bus fault, the following error message appears:

No bus error when user access I/O address X

User I/O Interrupt Test Screen Display

```
USER I/O INTERRUPT TEST
     USER I/O INTERRUPT SUBTEST 1
     USER I/O INTERRUPT SUBTEST 2
```

Clock Test

This test sets up a clock interrupt so that a digit appears on the screen every second and counts down from 9. The screen shows 9, 8, 7, 6, ..., 1.

The following error message may appear during the clock test:

```
Time out while waiting for 60 Hz interrupt
```

Clock Test Screen Display

```
CLOCK TEST
     Subtest 1 - Timer 1/Counter 2 TEST
          9 8 7 6 5 4 3 2 1 0
```

Printer Test

The printer test has two parts. First the status register is read, and then a barber pole printing pattern is sent to the printer.

Printer Test Screen Display

```
LINE PRINTER TEST
     LINE PRINTER SUBTEST 1, Status test
Line printer is selected.
     LINE PRINTER SUBTEST 2, Transfer test
Line printer is selected.
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

Communications Test

This test does a loopback test and checks combinations of different baud rates, number of bits, and types of parity as listed below:

- Baud rate is 300, 1200, 2400, 4800, 9600, or 19,200
- Bit count is 5, 6, 7, or 8
- Parity is none, odd, or even

Communications Test Error Messages

```
Overrun error
Framing error
Parity and framing error
```

Communications Test Screen Display

```
COMMUNICATION TEST (Self-test & Transfer test)

SELF-TEST
TRANSFER TEST

300 Baud
7 bits/character    no parity
7 bits/character    odd parity
7 bits/character    even parity
8 bits/character    no parity

1200 Baud
7 bits/character    no parity
7 bits/character    odd parity
7 bits/character    even parity
8 bits/character    no parity

2400 Baud
7 bits/character    no parity
7 bits/character    odd parity
7 bits/character    even parity
8 bits/character    no parity

4800 Baud
7 bits/character    no parity
7 bits/character    odd parity
7 bits/character    even parity
8 bits/character    no parity

9600 Baud
7 bits/character    no parity
7 bits/character    odd parity
7 bits/character    even parity
8 bits/character    no parity

19200 Baud
7 bits/character    no parity
7 bits/character    odd parity
7 bits/character    even parity
8 bits/character    no parity
```

After 19,200 baud, the program returns to the main diagnostics menu.

Modem Test

During this test, an internal loopback test sequence checks all possible combinations of the following parameters:

- 300 or 1200 baud
- 7- or 8-bit characters
- No parity, odd parity, or even parity

Modem Test Error Messages

```
SELF TEST failure detected
MODEM TRANSFER TEST, receive error - parity error,
     expected XX
```

Modem Test Screen Display

```
MODEM TEST (Self-test & Transfer test)
     SELF-TEST(B212 mode) at 300 baud..
          Test passed with no error detected.
     SELF-TEST (B212 mode) at 1200 baud..
          Test passed with no error detected.

     DATA TRANSFER TEST at 300 baud..
7 bits/character              no parity
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********

7 bits/character              odd parity
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********

7 bits/character              even parity
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********

8 bits/character              no parity
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********
******** ******** ******** ******** ******** ********
```

4 Logic Board Test Procedures

This section is a collection of test procedures for component-level troubleshooting of the **UNIX** PC logic board. In addition to standard test equipment, the following items are required:

- A set of debugger EPROMs
- A set of map RAM test EPROMs
- A set of RAM test EPROMs
- A set of silent loader EPROMs
- A logic analyzer
- An unintelligent terminal
- A master set of PALs
- A supply of the three semicustom gate arrays

The following reference books will also be useful:

- Motorola's MC68010 16-Bit Virtual Memory Microprocessor
- Motorola's MC68000 Programmer's Reference Manual
- Western Digital's Storage Management Products Handbook
- Intel's Microprocessor and Peripheral Handbook

Information provided with the board usually indicates to an experienced technician the tests that should be used. If the nature of the problem is not known, however, the first step in troubleshooting is to determine the highest level of diagnostics that will run. The higher the level, the larger the portion of the board that must be working and thus can be ruled out as the cause of the problem. Procedures associated with that level are then used to pinpoint the cause of the problem. (Some of these procedures have training value as well as testing value, so it is recommended that they be practiced on a known good board.)

The diagnostic levels are listed below in ascending order:

- Map RAM EPROM
- RAM EPROM
- Silent loader
- Debugger program
- Floppy disk diagnostics

MAP RAM EPROM Program

The map RAM EPROM program executes the following tasks:

- Performs data test
- Performs address test

Data Test

The map RAM EPROM tests the map RAMs and outputs data to the LEDs as listed in Table 4-1, (LED 4 is the one nearest the corner of the board):

Table 4-1 Logic Board LED States

Function	LED 4	LED 3	LED 2	LED 1
Testing data	On	Off	Off	Off
Testing address	On	On	Off	Off
Data error	On	Off	Off	On
Address error	On	On	On	Off

If a data error pattern appears, the EPROM is executing a loop that continuously reads and writes to an address where the data read back differs from the data written. This memory cycle can be observed using a logic analyzer. Set the analyzer to trace from the beginning of this loop. In the EPROM currently being used, this loop is located at 80007A hexadecimal, the address of the first instruction in the loop. The loop contains the following assembly instructions:

```
1$    MOVEW     D1,A0@
      MOVEW     A0@,D0
JMP   1$
```

The MOVEW instruction moves a 16-bit word from internal 68010 register D1 to the memory location whose address is contained in 68010 address register A0. Thus the first instruction is a memory write instruction. The second instruction is similar except that it reads from memory to register D0. The third instruction is a jump that causes the first instruction to repeat. Thus, once this loop is entered, these instructions will repeat as long as the power is on.

When the logic analyzer is set to trace starting at the location of the first instruction, it shows the address and data that were written during the first instruction and read during the second. The data read must differ from the data written for the program to have entered the loop. An example of address and data follows:

Address	Data	Type of Cycle
400000	0000	Data write
400000	0800	Data read

In this example, data bit D11 is a 0 during a write and a 1 during a read. Each static RAM chip contributes 4 bits to the data bus. The bit assignment is as follows:

Data Bits	SRAM Reference Designator
D08 & D13-D15	19C
D12-D09	20C
D04-D07	22C
D00-D03	21C

For the example above where D11 fails, device 20C is the most likely cause. Other causes could be the 74F245 buffers which connect the system data bus (D00-D15) with the static RAM data pins. Also, a bit stuck at 1 or at 0 at the first memory location, address 400000 could be caused by the static RAM and the buffers. A bit stuck at only one address (400020 for instance) and no others, suggests the static RAM and not on the buffer is at fault since its data bit is correct for other addresses.

Address Test

In the address test, the program first writes various data to all memory locations. It then checks all memory to see if there are any locations that do not have proper data. If an address line is faulty, shorted, open, or has some other problem, the program assumes that, at some point in the process of writing to all locations, a write in some location (call it new) changes the contents of a previous location (call it old). When it reads all locations and finds one that is incorrect, the program considers this location to be old. The old location is stored.

The next phase of the test determines the new location. To do this, the program starts a second writing operation to all memory locations. Each time it does a write, the program checks the old location to see if the contents have changed. When the program detects a change in the contents of the old address, it stores the address written to, because this must be new.

Error Loops

The following tables show the addresses of machine code that executes when the map RAM EPROM program finds an address or data error. These serve as trace addresses when a logic analyzer is used to determine the error addresses and data.

Data error (LEDs 1 and 4 on; LEDs 2 and 3 off):

Address	Register Notation	Description
800084:	MOVW D1, (A0)	Writes contents of D1 to address in A0
800086:	MOVW (A0), D0	Reads contents of address in A0
800088:	JMP 800084	Returns to top of loop

Both error addresses found (LEDs 4, 3, and 2 on; LED 1 off):

Address	Register Notation	Description
8000FA:	MOVW (A4), D0	Reads memory address in A4
8000FC:	MOVW D3, (A4)	Writes to memory; A4 holds address that causes contents of memory address in A0 to change when it is written to
8000FE:	MOVW (A0), D0	Reads memory address in A0
800100:	MOVW D7, (A0)	Writes to address in A0
800102:	JMP 8000FA	Returns to top of loop

Second error address not found (LEDs 4, 3, 2 on; LED 1 off):

If an address error occurs but the program cannot find the second error address, the following instruction loop is entered:

```
800110:   MOVW (A0), A0
800112:   JMP 800110
```

Data failures for data bits D10-D15 will be found in the address test instead of the data test as these bits are not fully exercised in the data test.

RAM EPROM Program

The RAM EPROM program executes the following tasks after setting unity map:

- Performs data test
- Performs address test

Data Test

The program performs a walking ones and walking zeros test of 512KB of memory. Each address is written to and then the contents are read back. If the contents read differ from those written, the program jumps to the data error loop.

Address Test

The address test of RAM is similar to the test of map RAM above except that several different data patterns are written. First a data pattern of 0-256 is written to all memory addresses. Then memory is divided into eight 64K blocks. Each block is then tested by dividing it into 256 subblocks of 256 bytes each and writing a different data word to each subblock. As in the map RAM address test, there are two error loops, one when both error addresses have been found and one when the second address cannot be found.

Error Loops

The following addresses are for machine code that executes when the RAM EPROM program finds an address or data error. These serve as trace addresses when a logic analyzer is used to determine the error addresses and data.

Data error loop (LEDs 1 and 4 on; LEDs 2 and 3 off):

```
8000A4:   MOVW D1, (A0)
8000A6:   MOVW (A0), D0
8000A8:   JMP 8000A4
```

Both error addresses found (LEDs 4, 3, 2 on; LED 1 off):

```
8001EE:   MOVB (A4), D0
8001F0:   MOVB D3, (A4)
8001F2:   MOVB (A1), D0
8001F4:   MOVB D7, (A1)
8001F6:   BRA 8001EE
```

Second error address not found (LEDs 4, 3, 2 on; LED 1 off):

```
800202:   MOVB (A1), D0
800204:   BRAL 800202
```

Debugger Program

The debugger is a breakpoint monitor program. With the debugger, the user can modify memory and run programs. That is, the user can enter and run programs, disassemble instructions, and set breakpoints. The debugger includes a load command that allows downloading diagnostics into memory from another computer. This can be used to load diagnostics from a machine that can load diagnostics from a floppy into one that cannot.

To set up the debugger program:

1 Replace the boot ROMs with the debugger ROMs.

2 Connect the **UNIX** PC to an unintelligent terminal using the RS-232-C port.

3 Push the Reset button.

The following message appears:

```
S4      MC68010      ROM      DEBUGGER      V1.0

COPYRIGHT 1984 BY CONVERGENT TECHNOLOGIES INC.

SR=XXXXXXXX PC=00800F66 SP=00800F66 UP=XXXXXXXX
D0=XXXXXXXX D1=XXXXXXXX D2=XXXXXXXX D3=XXXXXXXX
D4=XXXXXXXX D5=XXXXXXXX D6=XXXXXXXX D7=XXXXXXXX
A0=XXXXXXXX A1=XXXXXXXX A2=XXXXXXXX A3=XXXXXXXX
A4=XXXXXXXX A5=XXXXXXXX A6=XXXXXXXX A7=XXXXXXXX
00800F66         bras    0x00800F64
DBG>
```

The program counter (PC) shows the address of the next instruction to be executed. SP and UP are supervisory and user stack pointers, respectively, D0-D7 are data registers, A0-A7 are address registers, and SR is the status register.

After the debugger (DBG>) prompt, type **he** (for the Help command). The following message appears, listing the debugger program commands:

COMMANDS: BR, BC, BO, DB, DF, DI, DM, DR, DW, GO, HE, LO, MB, MM, MR, MW, WM, WW, WB, TR

These commands are entered after the DBG> prompt is displayed. The first group, the breakpoint group, consists of BR and BC. BR followed by an address sets a breakpoint at that address; BC followed by an address clears the breakpoint at that address.

For example, to set and clear a breakpoint at address 40000:

1 After the DBG> prompt, type **br 40000** and press <Return>.

The following message appears:

1 BREAKPOINTS SET AT: 00040000

2 Type **bc 40000** and press <Return> to clear the breakpoint.

Using the debugger ROMs, you can set and clear as many breakpoints as necessary depending on your application. If you try to clear a breakpoint at an address where one does not exist, the following message appears:

NO BPT AT THAT ADDR

When a program containing several breakpoints stops at any given breakpoint, type **go** and press <Return> after the DBG> prompt to continue program execution to the next breakpoint.

The next group of commands, the display group, includes DB, DF, DM, DR, and DW. When followed by an address, command DB (display byte) causes the next 16 bytes of data to be displayed. Pressing <Return> causes 16 more bytes of data to be displayed; typing / and pressing <Return> recalls the DBG> prompt.

For example, to display 16 bytes starting at address 40000:

1 After the DBG> prompt, type **db 40000** and press <Return>.

The following message appears, displaying the 16 bytes:

00040000: XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX

2 Press <Return> again.

The screen displays the next 16 bytes:

00040010: XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX

3 Type / and press <Return> to recall the DBG> prompt.

The DF (display all registers) command presents all registers internal to the 68010. To use this command, simply type **df** and press <Return> to display all registers.

The DM (display 32-bit word) command, when followed by an address, displays the 32-bit word starting at that address. Pressing <Return> gives the next 32-bit word; typing / and pressing <Return> recalls the DBG> prompt.

The DR (display register) command displays each of the 68010 registers just as the DF command does.

The DW (display 16-bit word) command, when followed by an address, displays the 16-bit word located there. Pressing <Return> gives the next 16-bit word; typing / and pressing <Return> recalls the DBG> prompt.

The BO (boot the **UNIX** PC) command first checks to see if there is a bootable floppy inserted. If not, it boots from the hard disk.

The GO command, when followed by an address, causes program execution to begin at that address.

HE is the Help command, which has already been discussed.

LO, the Load command, downloads a program into memory from the RS-232-C port.

The next group of debugger commands, the modification group, includes MB, MM, MR, and MW. With this group, the user can inspect and change the contents of various addresses and registers in the **UNIX** PC.

The MB (modify byte) command, when followed by an address, displays the 16-bit word at that address and enables the user to modify the word. The least significant bit of the address indicates whether the upper or lower half of the 16-bit word can be modified. If it is clear (0), the upper half of the 16-bit word can be modified; if it is set (1), the lower half can be modified. Pressing <Return> allows the next byte to be modified; typing / and pressing <Return> recalls the DBG> prompt.

The MM (modify 32-bit word) command enables the user to modify an entire 32-bit word at a specified address. Pressing <Return> allows the next 32-bit word to be modified; typing / and pressing <Return> recalls the DBG> prompt.

The MR (modify register) command displays each of the 68010 registers so the user can find the one that needs to be modified. It then allows the user to modify that register. Pressing <Return> displays the next register; typing / and pressing <Return> recalls the DBG> prompt.

The MW (modify word) command lets the user modify the 16-bit word at the specified address. Pressing <Return> gives the next word; typing / and pressing <Return> recalls the DBG> prompt.

The write commands, including WM, WW, and WB, enable the user to change the contents of various addresses just as the modify commands do, but the write commands do not display the previous contents. Pressing <Return> lets you write to the next address; typing / and pressing <Return> recalls the DBG> prompt.

The TR (trace trap) command allows single-step execution through the user program. TR followed by an address starts the trace at that address.

Machine Language Programming

Table 4-2 on the next page, contains a few instructions for writing short programs, which can be loaded and run using the debugger program.

Definitions

Dn and An refer to address and data registers inside the 68010, where n is any number from 0 through 7. (An) refers to the contents of memory pointed to by the address in address register An.

Instructions consist of one op code word followed by extension words, if used.

2An in the op code instruction means 2 times the number of the address register. For example, to use the move instruction below (3/2An/8/Dn) to write the contents of data register D2 to the memory location contained in address register A1, the op code is 3282.

Table 4-2 Program Instructions

Machine Code	Register Notation	Description
3/2An/8/Dn	MOVE Dn to (An)	Writes contents of data register Dn to memory location contained in An.
3/2Dn/3/C [ext. word]	MOVE #word to Dn	Loads extension word into data register Dn.
2/2An/7/C [00XX]	MOVEA <ea>, An	Moves the two extension words into address register An. The first extension word contains the most significant address digits.
5/3/4/Dn	Dn = Dn - 1	Subtract Quick. Decrements data register Dn.
B/2Dn/7/C [immed. data]	CMP <ea>, Dn	Compares immediate data to Dn. Subtracts source operand from the specified data register and sets condition codes according to the result; the data register is not changed.

Table 4-2 Program Instructions (Continued)

Machine Code	Register Notation	Description
6/6/X/X	BNE <label>	Branch not equal. If this instruction is preceded by a CMP instruction (above) and the data words compared are not equal, then program execution continues at a location obtained by adding the displacement represented by <label> and the address of the next instruction. The displacement is a 2's complement form.
6/0/X/X	BRA <label>	Program execution continues at the address of the next instruction plus the displacement. The displacement is a 2's complement form.

To calculate the 2's complement displacement for a BNE or BRA instruction (see preceding table):

1 Count the number of bytes back to the opcode in the instruction that is to be branched to.

2 Convert this number to 2's complement by:

- Writing it as an 8-bit binary number
- Changing each 0 to 1 (binary 1's complement)
- Adding 1 (binary 2's complement)
- Converting to hexadecimal

Walking Ones Test Program

The following program sets a pattern of walking ones in the first 1/2KB of memory:

```
070000: 303C   MOVE 1h to D0
070002: 0001

070004: 307C   MOVEA 0100h to A0
070006: 0100

070008: 3100   MOVE D0, -(A0)  (loop)

07000A: E358   ROL D0

07000C: B0FC   CMPA (compare A0 with 0)
07000E: 0000

070010: 66F6   BNE (branch if not equal to loop)

070012: 4EF9   JMP (return to debugger)
070014: 0080
070016: 0EE0
```

Read/Write Loop Program

The use of an oscilloscope in troubleshooting the logic board is limited because most signals, such as address and data, do not have repeating waveforms that an oscilloscope can synchronize on. This problem can be solved with a short machine language program that continuously reads and writes the same address in an endless loop.

The program in Table 4-3 can be loaded into memory using the debugger memory write (MW) command and executed by typing go followed by the starting address of the program. Once the program is executing, an oscilloscope connected to a chip-select pin being addressed by the program synchronizes easily because the chip-select pulse repeats about every 2 micro-seconds. A second oscilloscope channel is used to measure logic levels on address and data lines when the chip-select is active.

To see how this works, execute the following procedure on a known good logic board. In this example, data 0F00, which turns off the LEDs, is written to address 4A0000.

1 Load the program shown below using the MW command.

I. C. VOLTAGE CHART

DEVICE	REFERENCE DESIGNATION	+5V	DGND	PAGE NO.
74F08	2ED, 25N	14	7	2,4,5,16,19,21
74F02	16M, 27N	14	7	3,4,5,16,17,22
74S03	18M	14	7	12
74LS04	5M	14	7	3,5,6,17,23
74F04	13M, 19F	14	7	2,4,12,16
74F08	4J, 28E, 28F, 24N	14	7	2,7,16,17,21,22
74LS08	28D, 28F	14	7	3,4,5,6,11,15,17
74LS10	13M	14	7	5,17
74F10	15M	14	7	12
74F11	27F	14	7	2,4
74LS14	4M, 18M	14	7	4,5,11,13,14
74F20	23C	14	7	2,21
74LS27	23D, 23M, 26M	14	7	2,6 & 16,21
74F32	3J, 13E, 21F, 24M, 24P, 26M	14	7	2,3,4,5,7,9,11,16,17,19,22
74S51	12M, 19M	14	7	3,17
74F64	18G	14	7	3
74LS74	25M, 27M, 28M	16	8	2,6,7,8,11,15
14F74	6M, 15M, 16M, 17M	14	7	4,12,17
74F86	26B	14	7	8,21,22
74S112	21E, 28G	16	8	3
74123	13N	16	8	12,24
74S124	14N	16	9	2
74LS138	26G, 27G, 28G	16	8	4
74F138	7J, 9J	16	8	17
74LS125	12F, 26M	16	8	3,11,13,16
74F139	6J	16	8	17
74F153	14M	16	8	12
74LS157	19M, 19N	16	8	14
74F175	18D, 18M	16	8	3,8
74LS240	17M, 24M	20	10	11,13,15
74LS244	9M, 15P, 16G, 24F, 25M, 26C	20	10	2,4,5,6,13,15,16,17,22
74F244	16F, 17F, 19G, 22D, 25G	20	10	2,3,5,13,18,22
74F245	18C, 12D, 13A, 13C, 13D, 17B, 19B, 28D, 21B, 23B, 23C, 24B, 24C	20	10	5,8,16,19,21
74F258	10J, 11F, 11G, 11H, 12E, 15B	16	8	17,18
74LS259	7M, 18M	16	8	4,6
74S260	27N	14	7	3
74LS273	17M, 27C	20	10	11,15
74S299	14B, 15D	14	7	8
74LS348	10F	16	8	6
74LS373	16D, 18C, 21D, 24D, 25D	20	10	6
74F373	17G, 23F	20	10	5,16
74F374	16M	20	10	2,3,6,12
74LS374	16F, 27B	20	10	15
74LS393	16E, 20D	14	7	7
74LS32	26F	14	7	4,5,8

I. C. VOLTAGE CHART

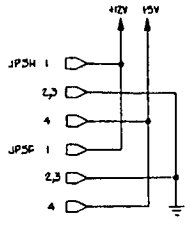
DEVICE	REFERENCE DESIGNATION	+5V	DGND	PAGE NO.
74LS31	14H	16	8	6,12,14
74LS32	15M	16	8	12
1488	21P ⚠2		7	14
1489	18P, 28P	14	7	14
2149	19C, 28C, 21C, 22C	18	9	16
2764/128	14C, 19C	28	14	3
6059	15G	12	1	14
4416	14A, 15A, 16A, 17A	5	18	8
4256	2E, 3E, 4E, 5E, 6E, 7E, 8E, 10E, 2F, 3F, 4F, 5F, 6F, 7F, 8F, 9F, 10F, 2G, 3G, 4G, 5G, 6G, 7G, 8G, 9G, 10G, 2H, 3H, 4H, 5H, 6H, 7H, 8H, 9H, 10H	8	16	19,20
68B18	14E	14,19	16,33	3
8356A	1B			24
8822A	2A			23
7281	21M	40	20	14
C5814	2A, 7A, 11M			23
DG281	5M			23
H11AA2	7N			23
LM324	2M			24
LM358	1D			24
LF412	17N			12
4N37	2P, 7P, 8M			23
PAL16L8A	24G	20	10	2
PAL16R4	14M	20	10	12
PAL16R4A	24H	20	10	2
PAL16R8A	25B	20	10	2
TC8250P	26D	N/A	8	15
WD1010-05	21H	40	20	11
WD2797	22M	21	20	12
75L05	1K			24
1805	1J			24
78L08	11N			24
78L05	2J			24
VIDEO ARRAY	17C	40	20	7
DMA DATA ARRAY	22H	20	40	10
DMA ADDRESS ARR	22E	20	40	9

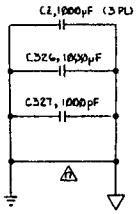
This divider is provided for your convenience.
Insert it before sections of the manual you use frequently.
Write an appropriate reference on the tab.

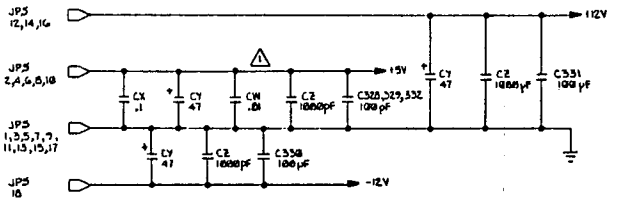
NOTES: UNLESS OTHERWISE SPECIFIED

1. CW CAPS ARE USED NEAR I.C.'S WITH 18 MHZ.
2. PIN 14 SHOULD CONNECT TO +12V; PIN 1 TO -12V
3. THESE GATES MUST BE IN THE SAME PACKAGE (PAGES 3, 16) ((LAYOUT))
4. ALL OUTPUT TRACES ON 74LS259 SHOULD BE AS SHORT AS POSSIBLE. (LAYOUT)
5. SHOULD BE A SHORT TRACE AND NO HIGH FREQUENCY TRACE NEARBY. (LAYOUT)
6. STUFFING OPTIONS: WITH 74S124 - STUFF R94 (NOT R95), C308 SHOULD BE 27pF
   WITH 74LS629 - STUFF R95 (NOT R94), C308 SHOULD BE 56pF
7. MPS 4258 IS AN ALTERNATE PART.
8. THESE COMPONENTS ARE ONLY TO BE STUFFED WHEN USING CONTROLLERS OTHER THAN NU2797.
9. DELETED
10. INSERT ONLY FOR 256K RAM CHIPS. ALSO CUT TRACE BETWEEN E2 AND E3 AND ADD JA1 FROM E1 TO E2.
11. THESE CAPACITORS SHOULD BE LOCATED NEXT TO T1 AND T2. (LAYOUT)
12. HEAVY TRACE LINES INDICATE 25 MIL TRACES, 50 MIL AIR GAP. (LAYOUT)
13. ALL 1/2 Ω RESISTORS SHOULD BE FUSEABLE AND NON-FLAMMABLE.
14. ALL 1/2W RESISTORS ARE TO BE NON-FLAMMABLE.
15. ⏚ INDICATES ANALOG GROUND.
16. ⏚ INDICATES DIGITAL GROUND.
17. DIGITAL AND ANALOG GROUND SHOULD ONLY BE CONNECTED AT SUPPLY ORIGIN. (LAYOUT)
18. ALL RELAYS ARE SHOWN AS DE-ACTIVATED.
19. CAPACITORS INDICATED SHOULD BE AS CLOSE TO I.C.'S AS POSSIBLE. (LAYOUT)
20. ⏚ INDICATES HAVING THE SHORTEST TRACE POSSIBLE BETWEEN THE COMPONENT AND ANALOG GROUND. (LAYOUT)
21. +12V AND -12V TO BE CONNECTED ONLY FROM SUPPLY ORIGIN. (LAYOUT)
22. SPEAKER MOUNTED ON MONITOR CASE.
23. ⏚ INDICATES CHASSIS GROUND.
24. ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.
25. ALL 1% RESISTORS ARE 1/4W.
26. CAPACITOR VALUES ARE IN MICROFARADS.
27. THESE COMPONENTS ARE TO BE DELETED WHEN USING 256K RAM'S FOR A ONE MEGABYTE SYSTEM.

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	CHK	APPROVED
	A	RELEASE TO CONTROL PER CO # 5199	10-31-84		
	B	REVISED PER C.O. # 5296	2-20-85		
	B	RELEASE TO MFG.	10-1-85		
	C	REVISED PER CO # 5331	10-7-85		
	D	REVISED PER CO # 5494	6-13-86		







REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C339	C1-39, 47-64, 67-87, 89, 93-151, 154-177, 182, 185-193, 199-235, 237, 238, 245, 247, 257, 259, 260, 261, 263, 274, 275, 278-283, 285-298, 300-302, 319-322, 324
CR20	
D1	
E9	E6, E7
F2	
H6	
L9	
Q15	
R146	R3, 18, 103-107, 111, 117, 125, 132-134
RP28	
SW1	
T2	
VR2	
Y1	
JA4	JP3

SPARE GATES		
DEVICE	REFERENCE DESIGNATION	QTY
26LS32	13A	1
74F10	13M	1
74F08	24N	3
74LS27	24N	2
74F244	25G	2
74S260	27N	1
74S112	21E	1
74S51	12H	1
74LS393	20D	1
74LS32	26F	2
LM 358	1D	1
1489	18P	1

INCHES

THIRD ANGLE PROJECTION

APPLICATION

DO NOT SCALE DRAWING

PARTS LIST

Convergent Technologies™

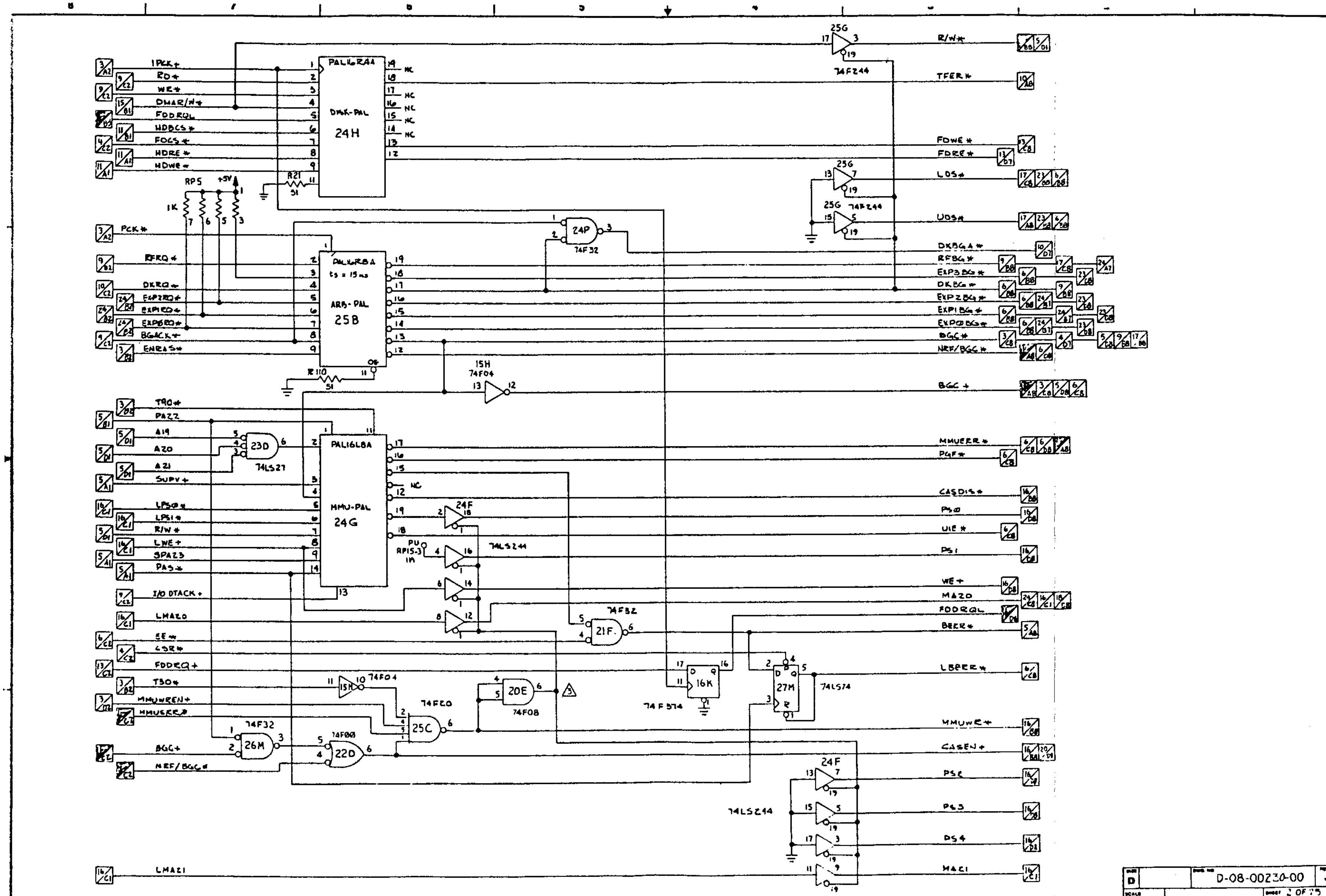
TITLE: SCHEMATIC : 54, CPU

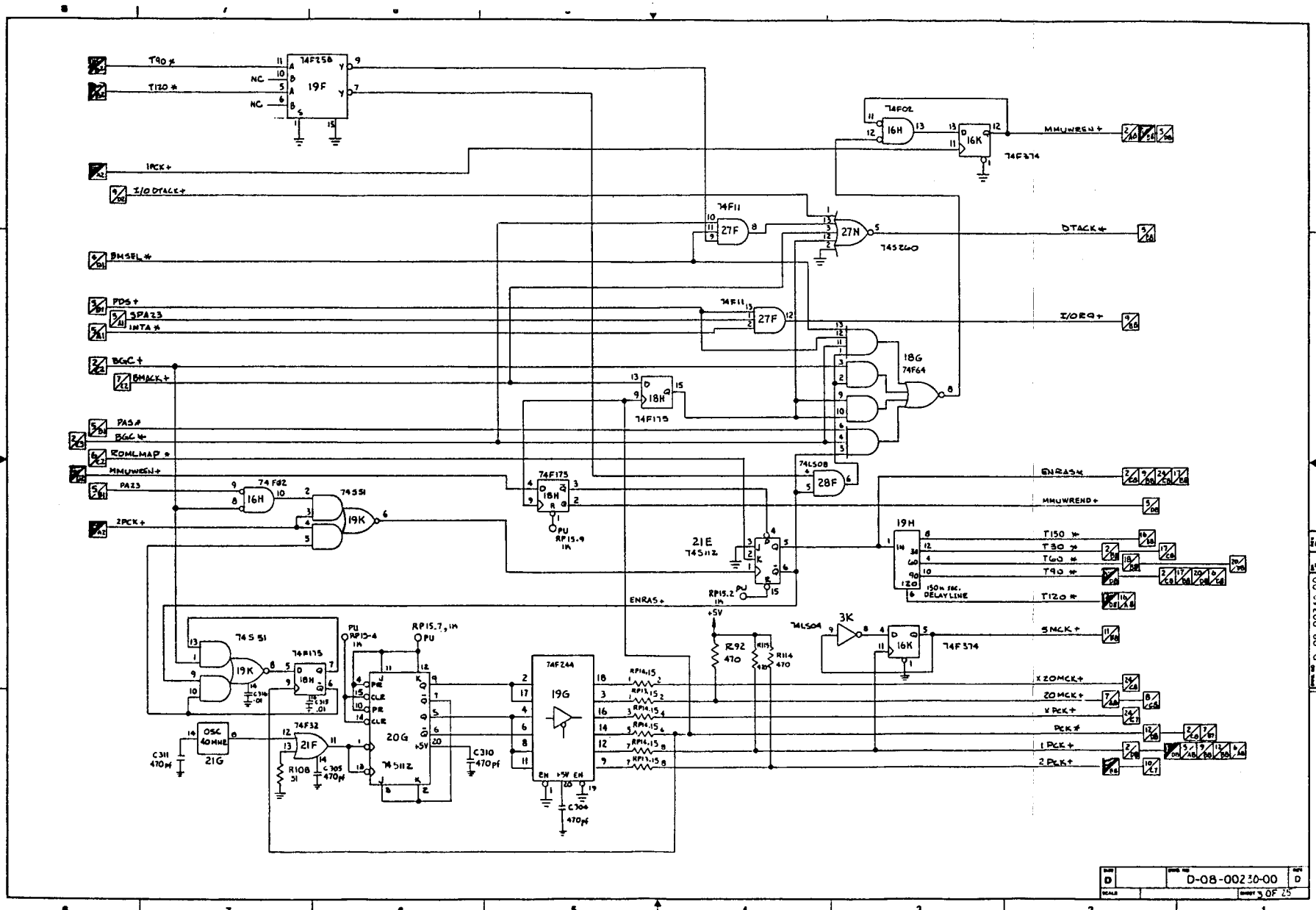
DRAWN	RAMA	1-3-85
CHECKED	BILL BLACK	1-9-85
APPROVED	DANIEL TAM	1-9-85

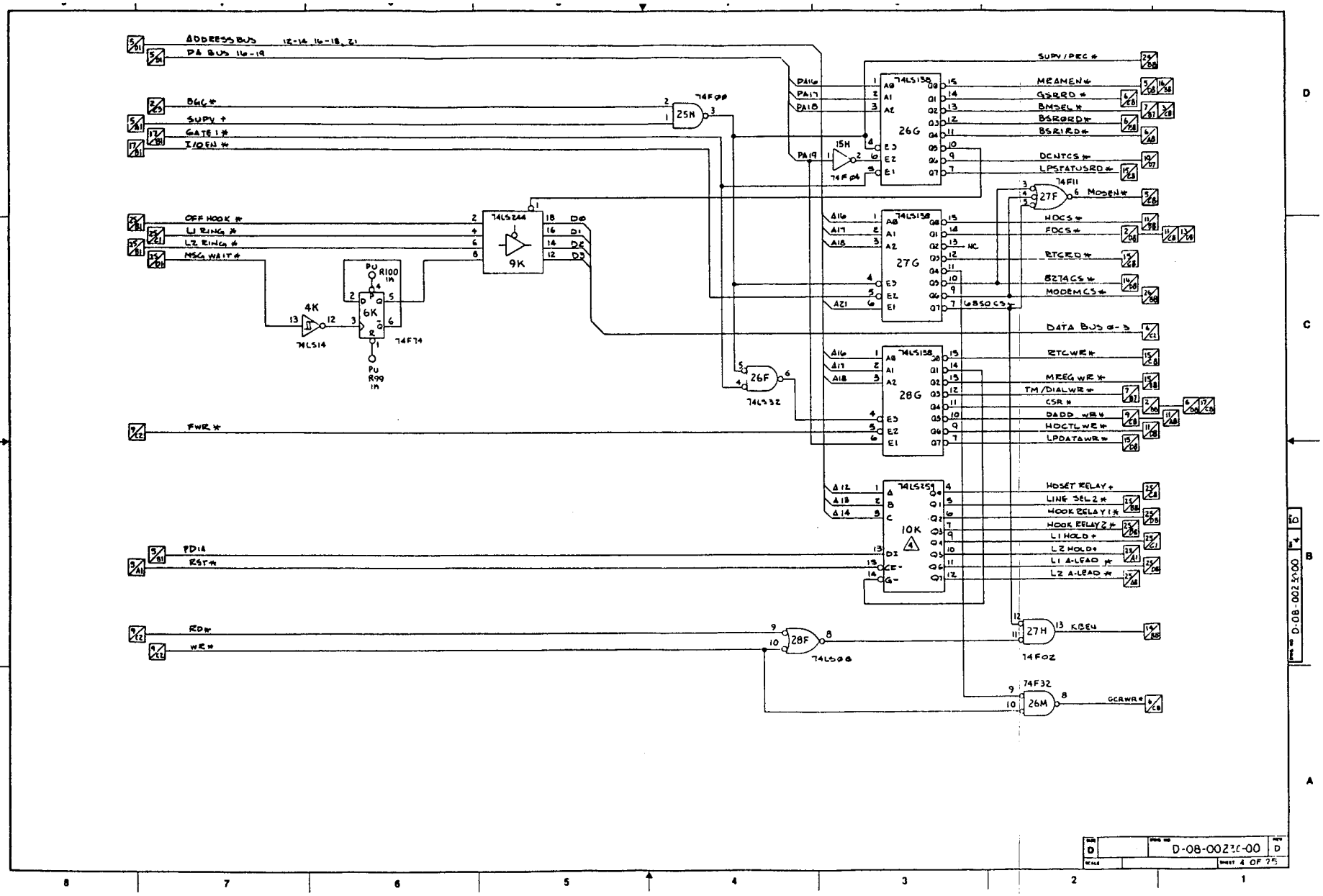
SIZE D | DRAWING NO. D-08-00230-00 | REV D

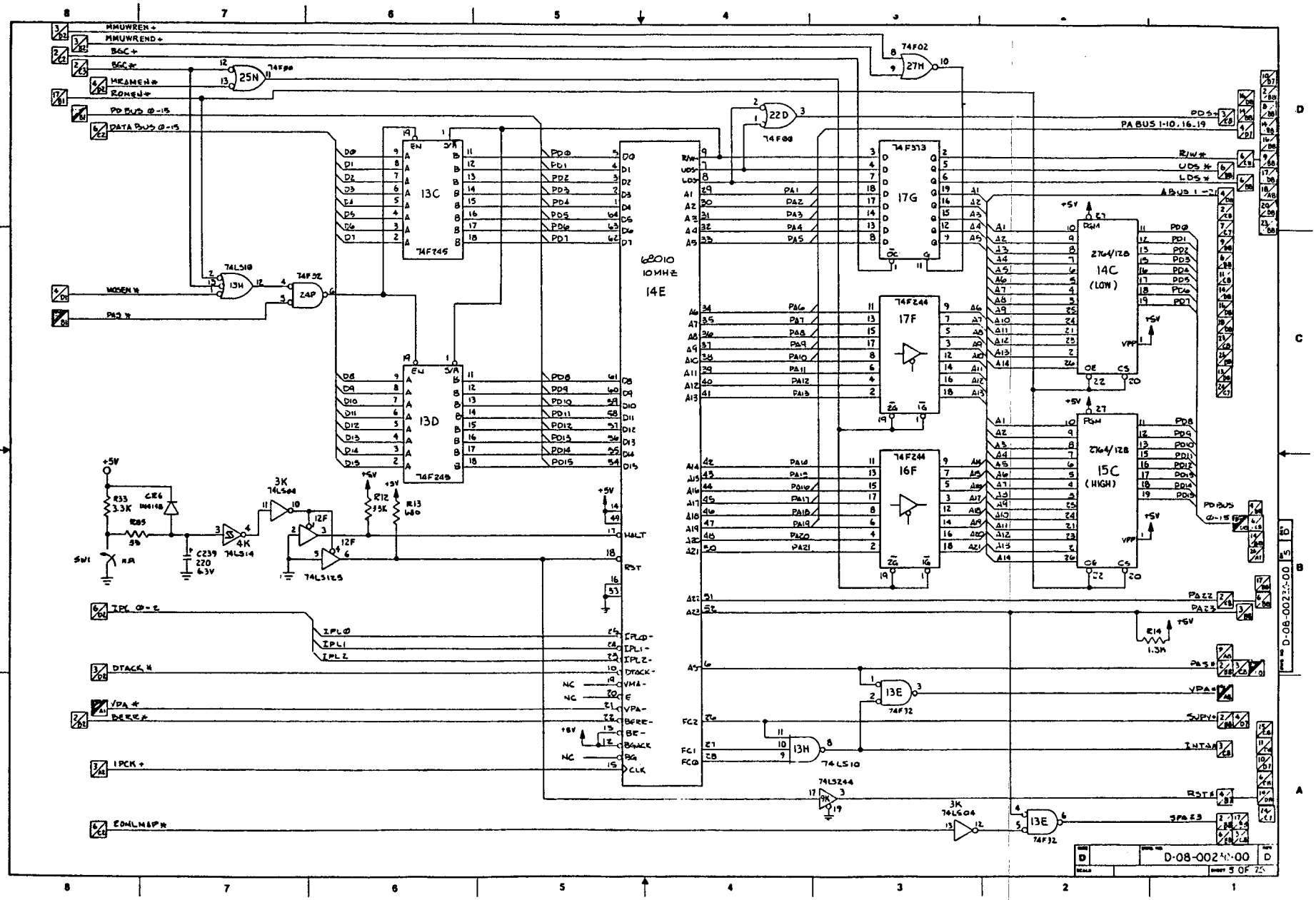
SCALE | SHEET 1 OF 15

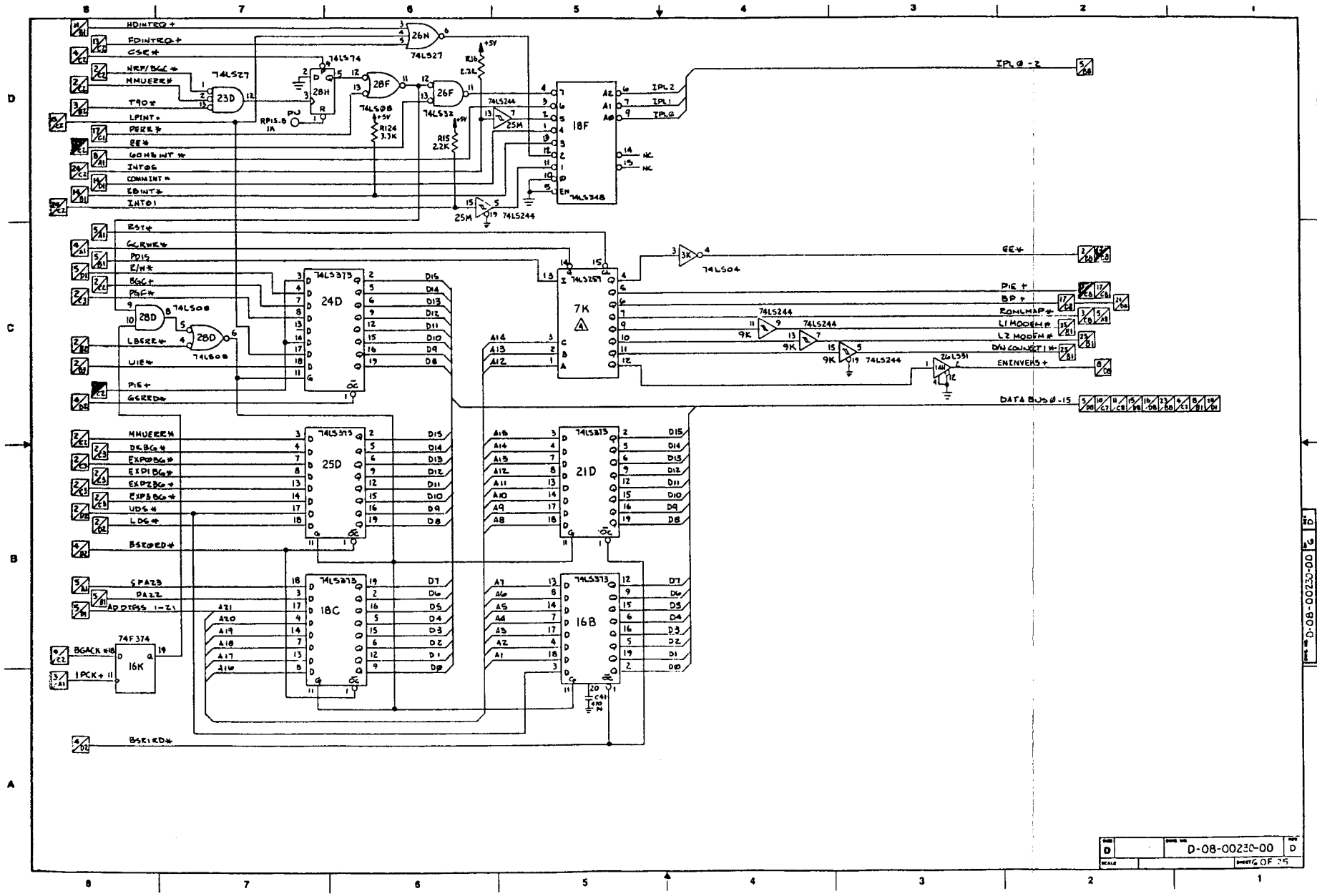
D-08-00230-00 C

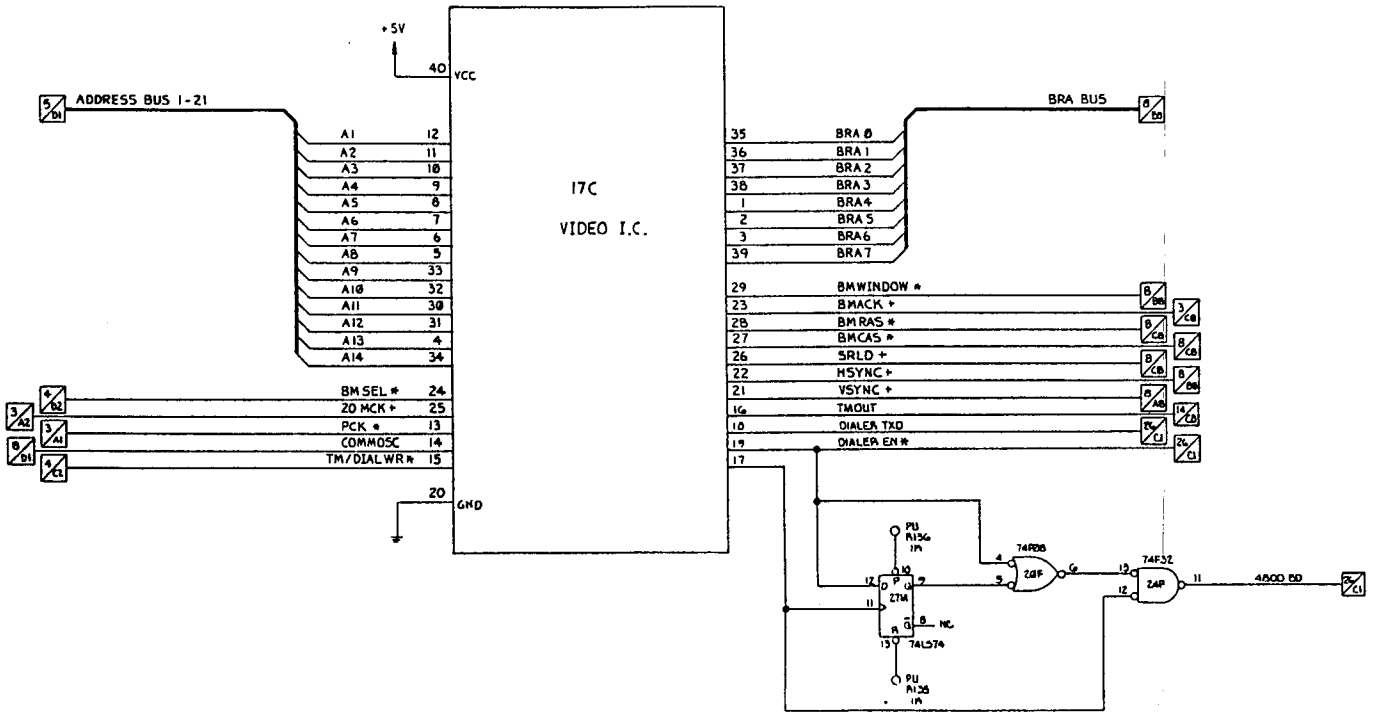

PAL16R4A
DMA-PAL
24H
PAL16R8A
ts = 15 ns
ARB-PAL
25B
PAL16L8A
MMU-PAL
24G
1PCK+
RD+
WE+
DMAR/W+
FDDRQL
HDBCS+
FDCS+
HDRE+
HDWE+
RP5
+5V
1K
R21
51
R110
PCK+
RFRQ+
DKRQ+
EXP2RQ+
EXP1RQ+
EXP0RQ+
BGACK+
ENRAS+
TRQ+
PA22
A19
A20
A21
SUPV+
LPS0+
LPS1+
R/W+
LWE+
SPA23
PAS+
I/O DTACK+
LMA20
SE+
LSR+
FDDRQ+
TSO+
MMUWREN+
MMUERR+
BGC+
NRF/BGC+
LMA21
25G
74F244
R/W+
TFER+
FDWE+
FDRE+
LDS+
UDS+
24P
74F32
DKBGA+
RFBG+
EXP3BG+
DKBG+
EXP2BG+
EXP1BG+
EXP0BG+
BGC+
NRF/BGC+
15H
74F04
BGC+
23D
74LS27
MMUERR+
PGF+
CASDIS+
PS0
UIE+
PS1
WE+
MA20
FDDRQL
BERR+
LBERR+
MMUWE+
CASEN+
PSC
PS3
PS4
MAC1
24F
74LS244
RP15-3
21F
74F32
16K
74F574
27M
74LS74
20E
74F08
25C
74F20
26M
74F32
22D
74F00
D
D-08-00230-00
2 OF 25


T90 *
T120 *
NC
NC
74F258
19F
IRCK+
I/O DTACK+
BMSEL *
PDS+
SPAZ3
INTA *
BGC+
BMACK+
PAS *
BGC *
ROMLMAP *
MMUWEN+
PA23
2PCK+
74F02
16H
16K
74F374
MMUWEN+
74F11
27F
27N
74S260
DTACK+
I/OEQ+
18G
74F64
18H
74F175
74LS08
28F
ENRAS+
MMUWREN0+
19H
T150 *
T30 *
T60 *
T90 *
T120 *
150n sec. DELAY LINE
21E
74S112
74S51
19K
74F32
21F
OSC 40MHz
21G
20G
74F244
19G
3K
74LS04
SMCK+
X20MCK+
20MCK+
XPCK+
PCK *
1PCK+
2PCK+
R92 470
R115 470
R114 470
C311 470pf
C310 470pf
C309 470pf
C305 470pf
C304 470pf
R108 51
+5V
PU
RP15.9 1K
RP15.2 1K
RP15-4 1K
RP15.7, 1K
RP14,15
D-08-00230-00
3 OF 25


ADDRESS BUS 12-14, 16-18, 21
PA BUS 16-19
B&G *
SUPV +
GATE1 *
I/OEN *
OFF HOOK *
L1 RING *
L2 RING *
MSG WAIT *
FWR *
FD18
RST *
RD *
WR *
74F08
25H
74LS244
9K
4K
74LS14
6K
74F74
R100 1%
R99 1%
26F
74LS32
74LS158
26G
15H
74F04
27G
28G
74LS259
10K
28F
74LS08
27F
74F11
27H
74F02
26M
74F32
SUPV/PEC *
MRAMEN *
GSRRD *
BMSEL *
BSRRD *
BSRIRD *
DCNTCS *
LPSTATUSRD *
MODEM *
HDCS *
FDCS *
RTCRD *
BZTACS *
MODEMCS *
6850CS *
DATA BUS 0-3
RTCWR *
MREG WR *
TM/DIALWR *
CSR *
DADD WR *
HDCTLWR *
LPDATAWR *
HDSET RELAY +
LINE SEL 2 *
HOOK RELAY 1 *
HOOK RELAY 2 *
L1 HOLD +
L2 HOLD +
L1 A-LEAD *
L2 A-LEAD *
K1BEN
GCRWR *
NC
D-08-00230-00
SHEET 4 OF 25

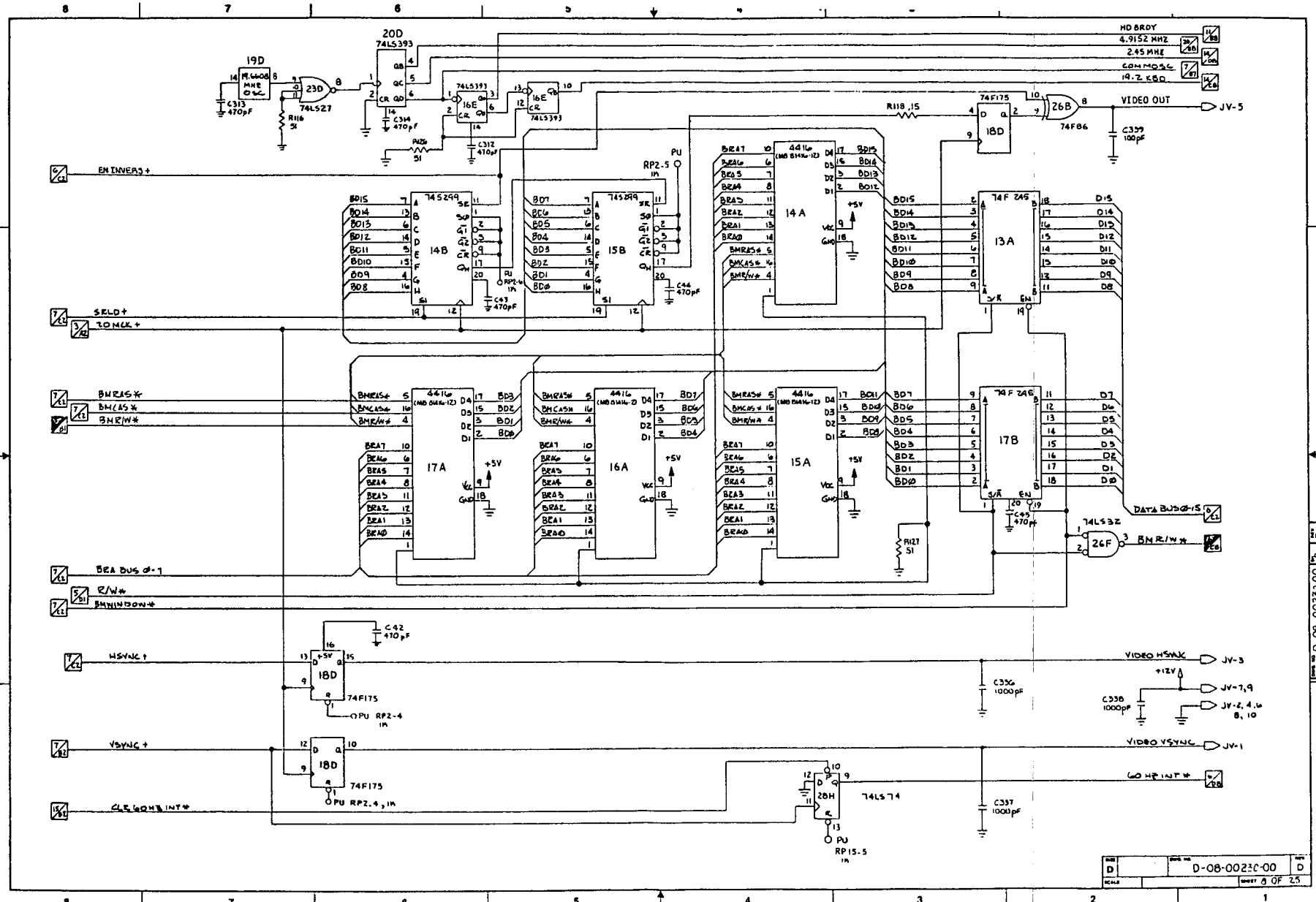

MMUWREN+
MMUWREND+
BGC+
BGC*
MEMEN*
RONEW*
PD BUS 0-15
DATA BUS 0-15
MOSEN*
PRO*
25N
74F08
27H
74F02
22D
74F08
13C
74F245
13D
74F245
13H
74LS10
ZAP
74F32
68010
10MHz
14E
17G
74F373
17F
74F244
16F
74F244
14C
(LOW)
2764/128
15C
(HIGH)
2764/128
PA BUS 1-10,16,19
R/W*
UDS*
LDS*
PD BUS 0-15
+5V
R33
3.3K
R35
33
SW1
C239
220
6.3V
3K
74LS04
4K
74LS14
74LS125
R12
33K
R13
680
R14
1.3K
13E
74F32
74LS244
3K
74LS04
IPL 0-2
DTACK*
VPA*
BERR*
IPCK+
EOWLMSP*
HALT
RST
IPL0-
IPL1-
IPL2-
DTACK-
VMA-
E
VPA-
BERR-
BG-
BGACK
BG
CLK
FC2
FC1
FC0
PA22
PA23
PA23
VPA*
SUPV*
INTA*
RST*
SPACE3
D-08-002[illegible]-00
SHEET 5 OF 25

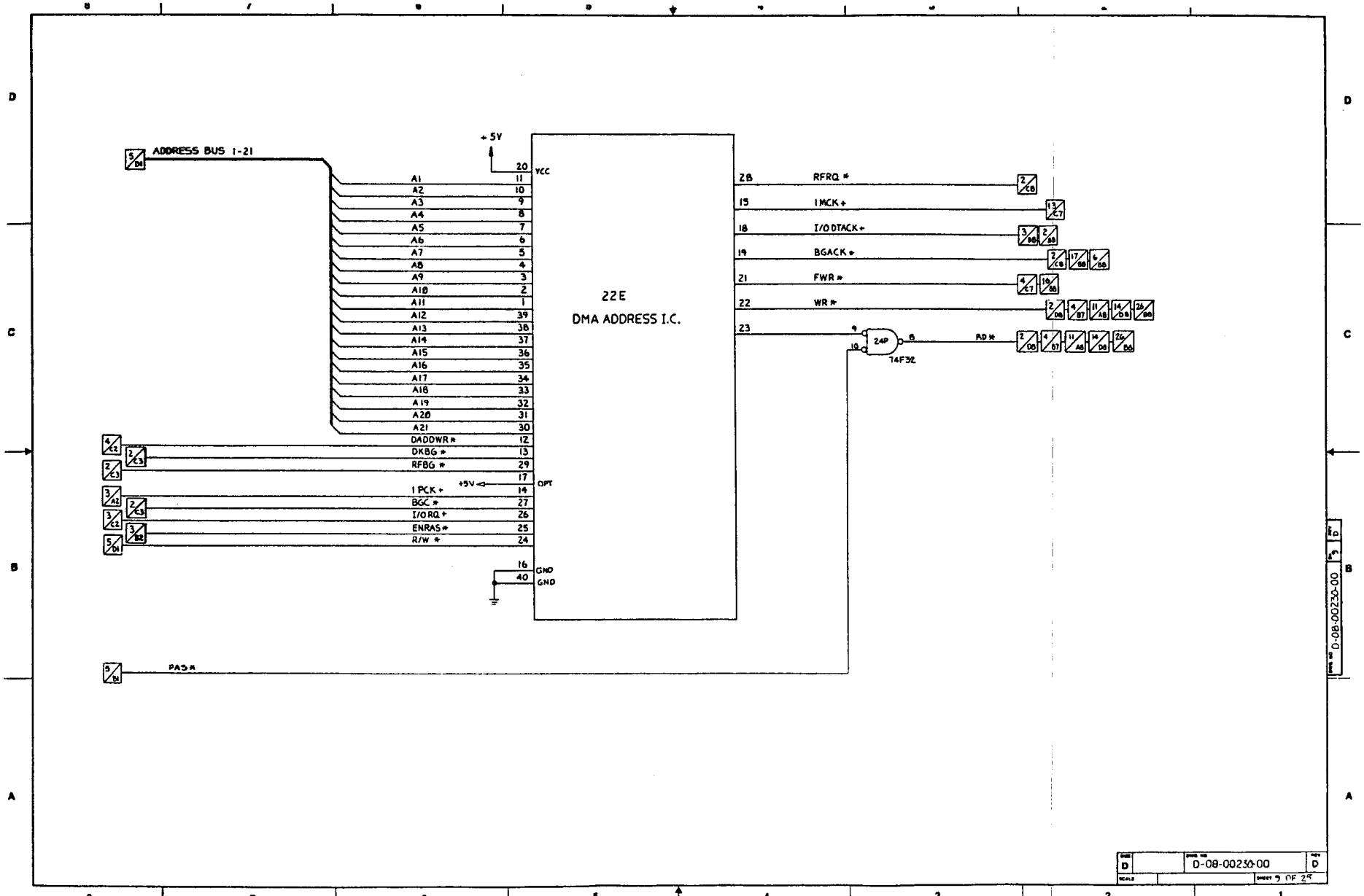

HDINTRQ+
FDINTRQ+
CSE*
NRF/BGC*
MMUERR*
T90*
LPINT+
PERR*
EE*
GOMBINT*
INT05
COMMINT*
KBINT*
INT01
26N
74LS27
74LS74
28H
28F
26F
74LS08
74LS32
74LS27
23D
RP15.0
1A
PU
+5V
R16 2.2K
R124 3.3K
R15 2.2K
74LS244
25M
18F
74LS348
IPL2
IPL1
IPL0
IPL@-2
NC
NC
EST*
GGRWE*
PDIS
R/W*
BGC+
PSEL*
28D
74LS08
LBERR*
UIE*
PIE+
GGRED*
24D
74LS373
7K
74LS259
3K
74LS04
EE*
PIE+
BP+
ROMLMAP*
L1 MODEM*
L2 MODEM*
DAI COMMIT1*
ENINVEN5+
9K
ZGL591
DATA BUS Ø-15
MMUERR*
DKBG*
EXPØBG*
EXP1BG*
EXP2BG*
EXP3BG*
UDS*
LDS*
BSTØED*
25D
21D
SPAZ3
PAZ2
ADDRESS 1-21
18C
16B
74F374
16K
BGACK*18
1PCK+11
BSTIRD*
D-08-00230-00
SHEET 6 OF 25

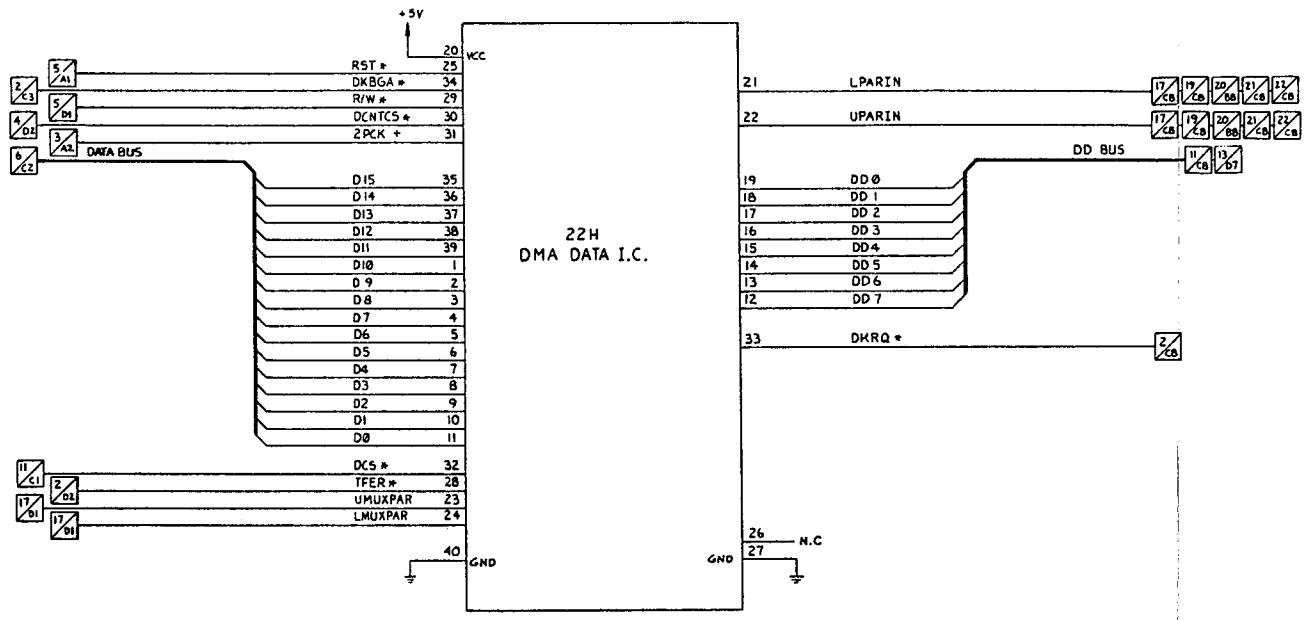


D-08-00230-00 D

SHEET 7 OF 27


HD BRDY
4.9152 MHZ
2.45 MHZ
COMMOSC
19.2 KBD
20D
74LS393
19D
74LS27
C313 470pF
C314 470pF
C312 470pF
R116 51
R120 51
16E
74LS393
RU18 ,15
74F175
18D
26B
74F86
VIDEO OUT
JV-5
C339 100pF
PU
RP2-5
1M
EN INVERS +
14B
74S299
15B
74S299
C43 470pF
C44 470pF
14A
4416
13A
74F 245
SELO +
ZONCK +
BMRAS*
BMCAS*
BMR/W*
17A
16A
15A
17B
C45 470pF
74LS32
26F
DATA BUS 0-15
BMR/W*
BEA BUS 0-7
R/W*
BMWINDOW*
C42 470pF
HSYNC +
VIDEO HSYNC
JV-3
C336 1000pF
+12V
C338 1000pF
JV-7,9
JV-2, 4, 6, 8, 10
VSYNC +
VIDEO VSYNC
JV-1
CLEGOMS INT*
74LS74
28H
GO MP INT*
C337 1000pF
PU RP15-5
1M
D-08-00230-00
SHEET 8 OF 25


ADDRESS BUS 1-21
+5V
22E
DMA ADDRESS I.C.
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
VCC
DADDWR *
DKBG *
RFBG *
OPT
I PCK +
BGC *
I/O RQ +
ENRAS *
R/W *
GND
GND
RFRQ *
IMCK +
I/O DTACK +
BGACK +
FWR *
WR *
AD *
74F32
PAS *
D-08-00230-00
SHEET 9 OF 24



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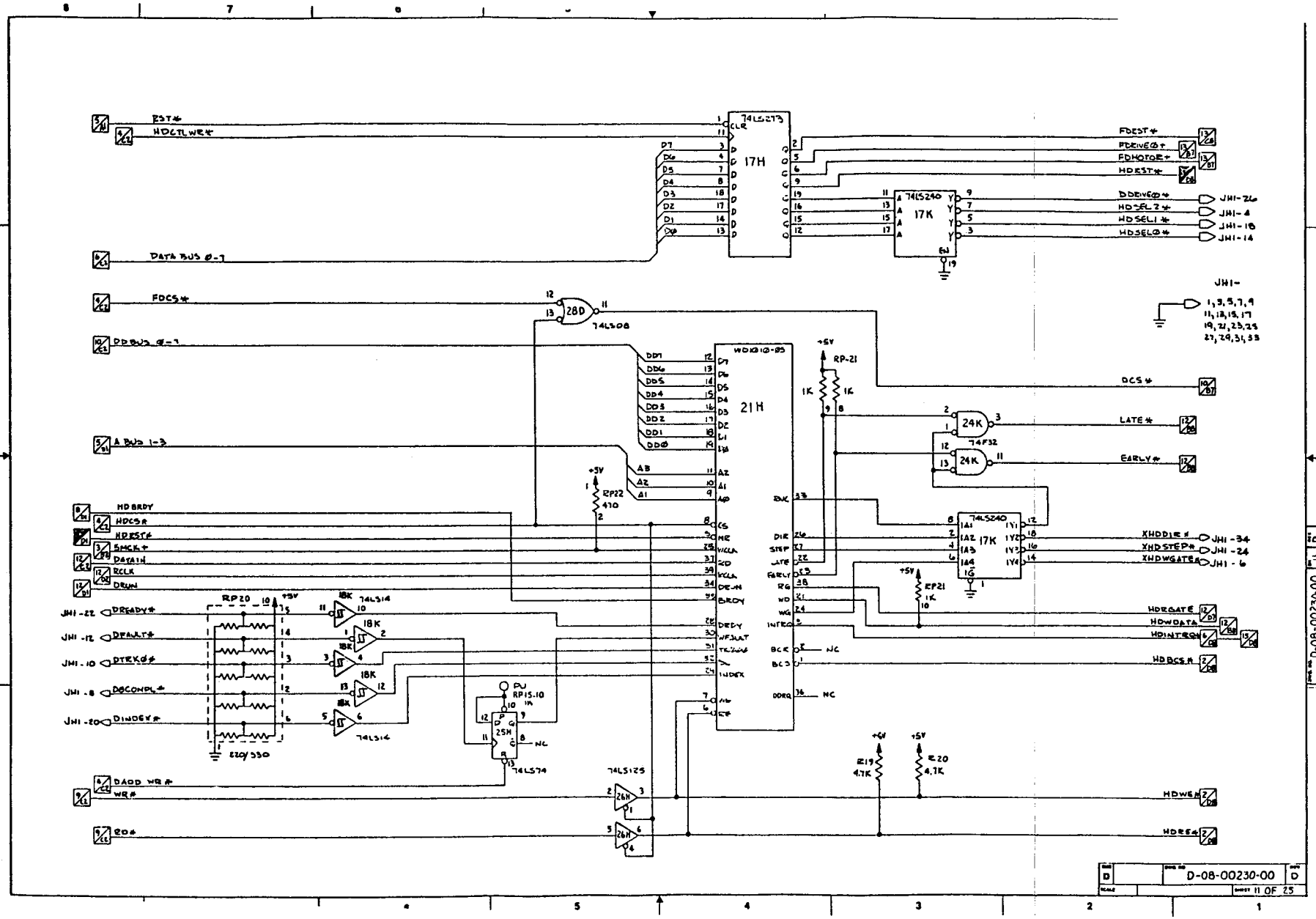
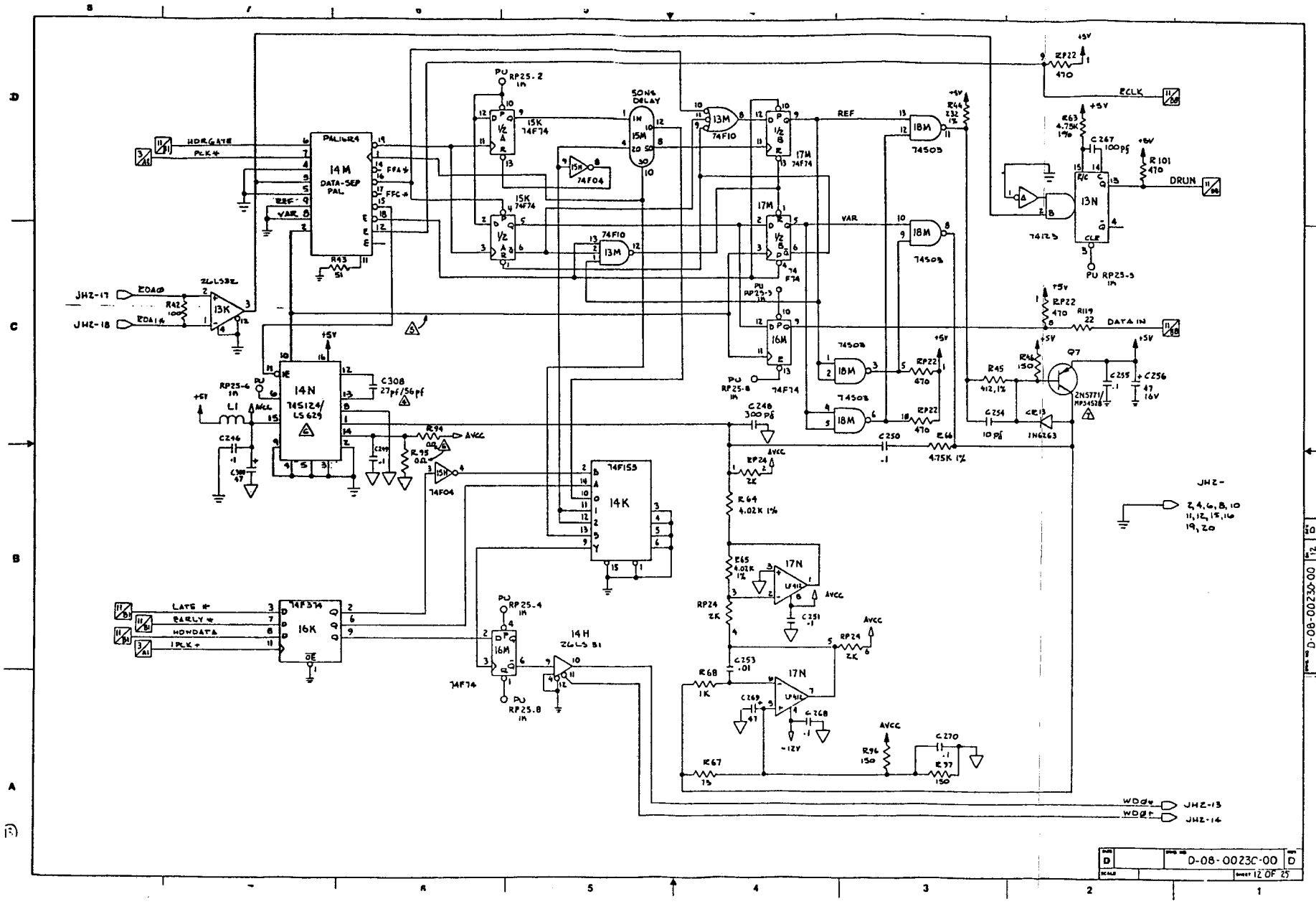
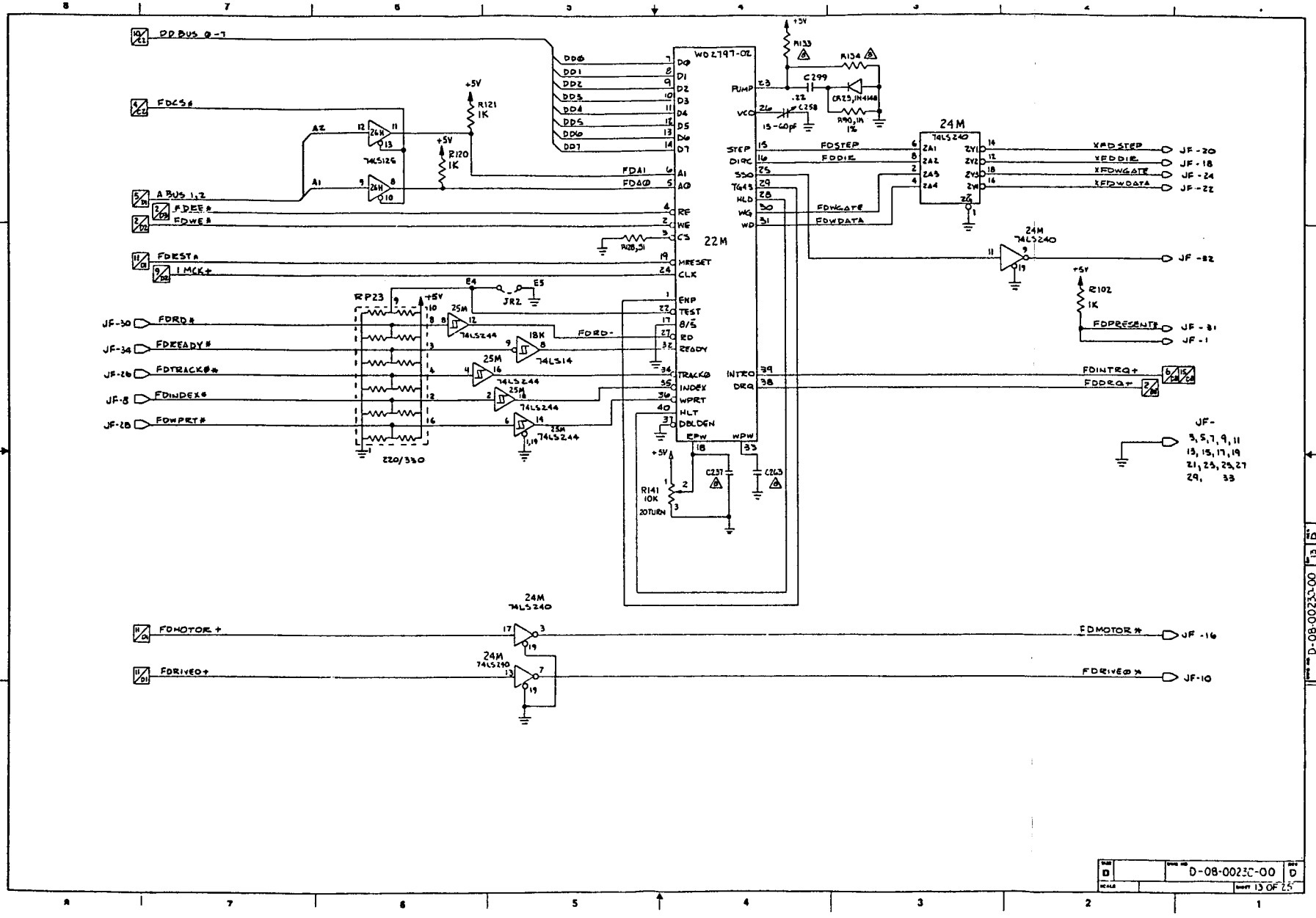
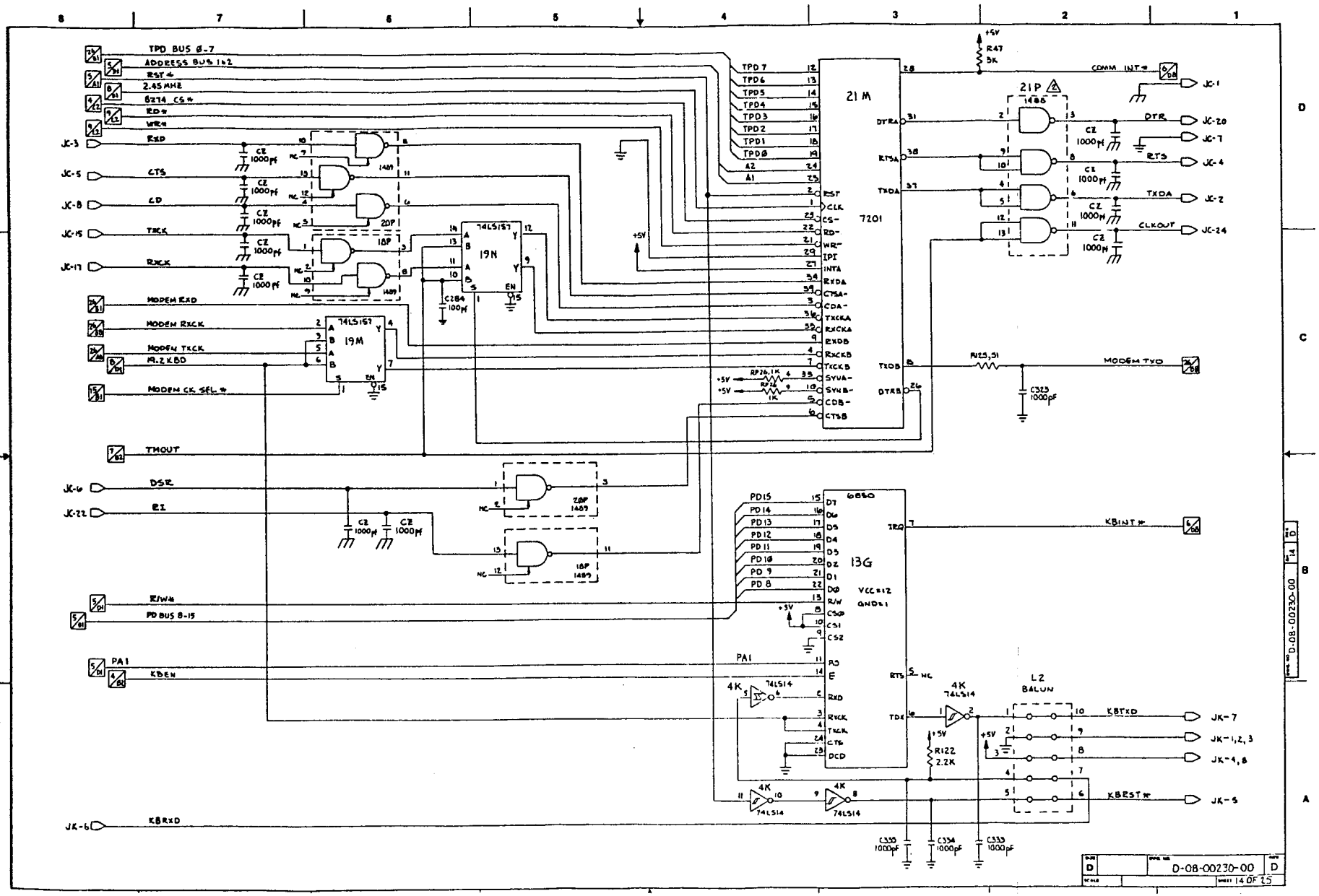
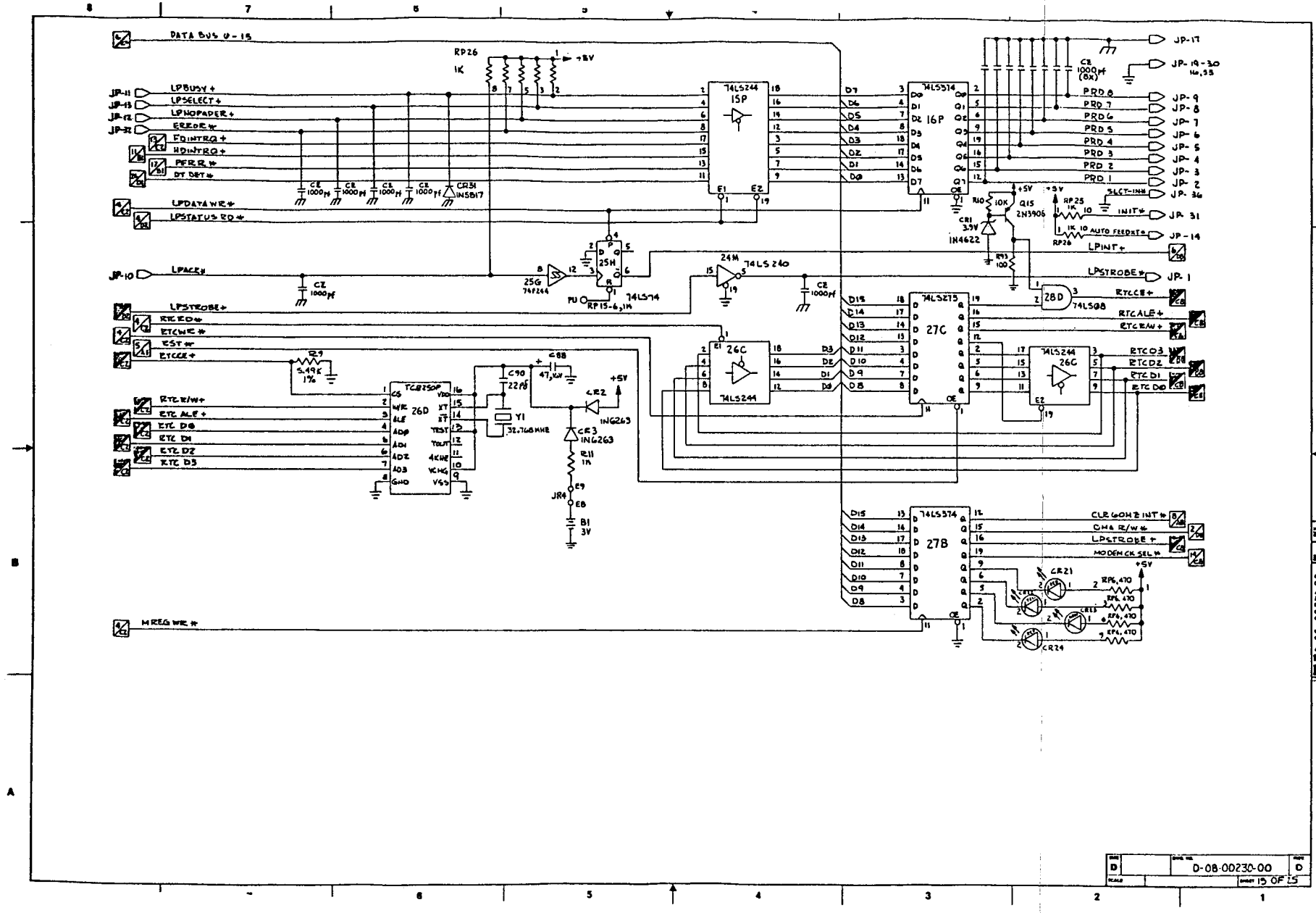
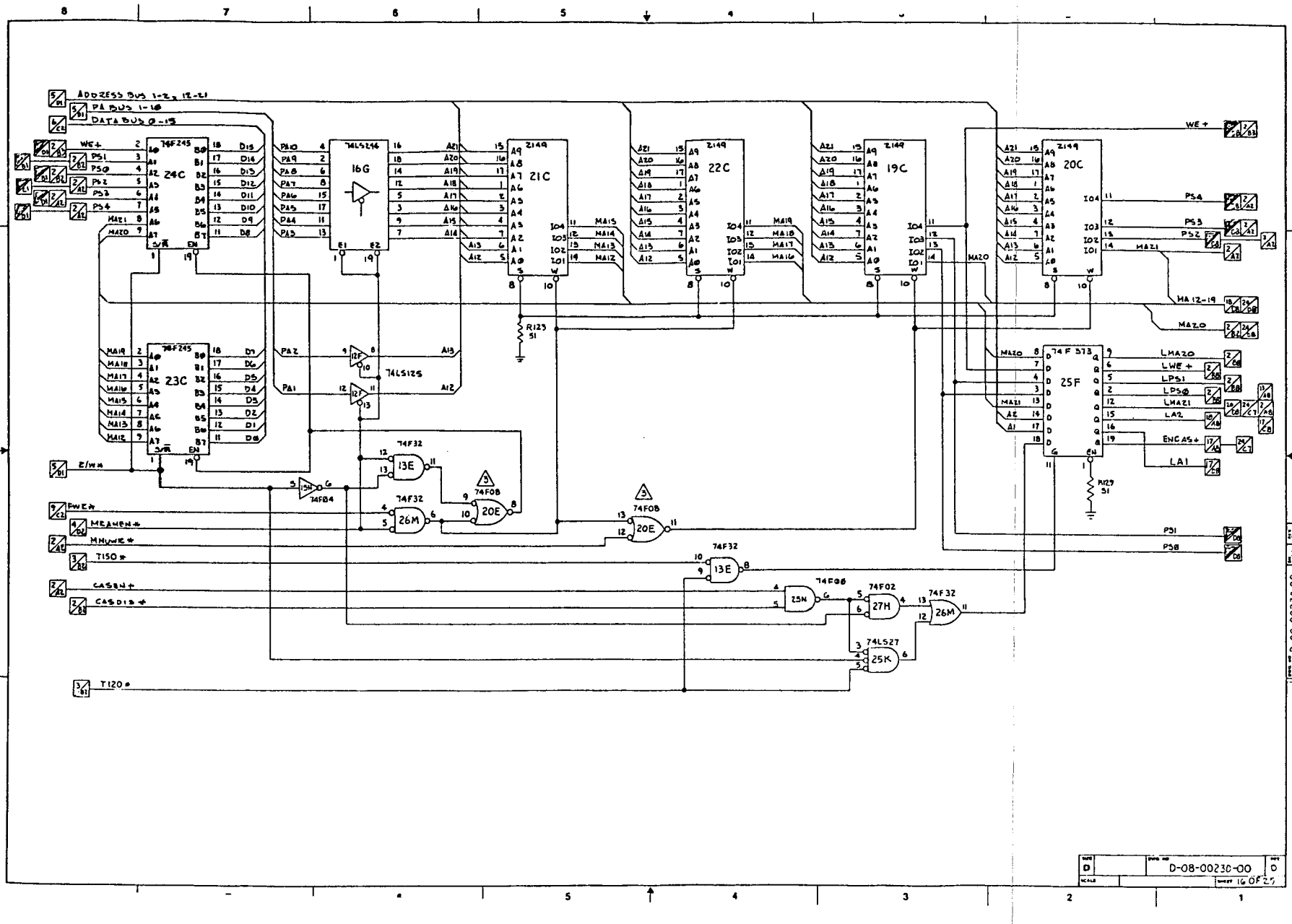

RST*
HDCTLWR*
DATA BUS 0-7
74LS273
17H
74LS240
17K
FDEST*
FDRIVE0*
FDMOTOR*
HDEST*
DDRIVE0*
HDSEL2*
HDSEL1*
HDSEL0*
JH1-26
JH1-4
JH1-18
JH1-14
JH1-
1,3,5,7,9
11,13,15,17
19,21,23,25
27,29,31,33
FDCS*
DDBUS 0-7
A BUS 1-3
74LS08
WD1010-05
21H
DCS*
LATE*
EARLY*
74F32
24K
RP-21
1K
RP22
470
HDBRDY
HDCS*
HDRST*
SMCK*
DATAIN
RCLK
DRUN
RP20
330
18K
74LS14
JH1-22 DREADY*
JH1-12 DFAULT*
JH1-10 DTRK0*
JH1-8 DSCOMPL*
JH1-20 DINDEX*
RP15-10
1K
74LS74
25H
74LS125
26H
DACK WR*
WR*
RD*
HDWEN
HDRE*
RP21
1K
R19
4.7K
R20
4.7K
XHDDIR*
XHDSTEP*
XHDWGATE
JH1-34
JH1-24
JH1-6
HDRGATE
HDWDATA
HDINTRQ*
HDDCS*
D-08-00230-00
SHEET 11 OF 25

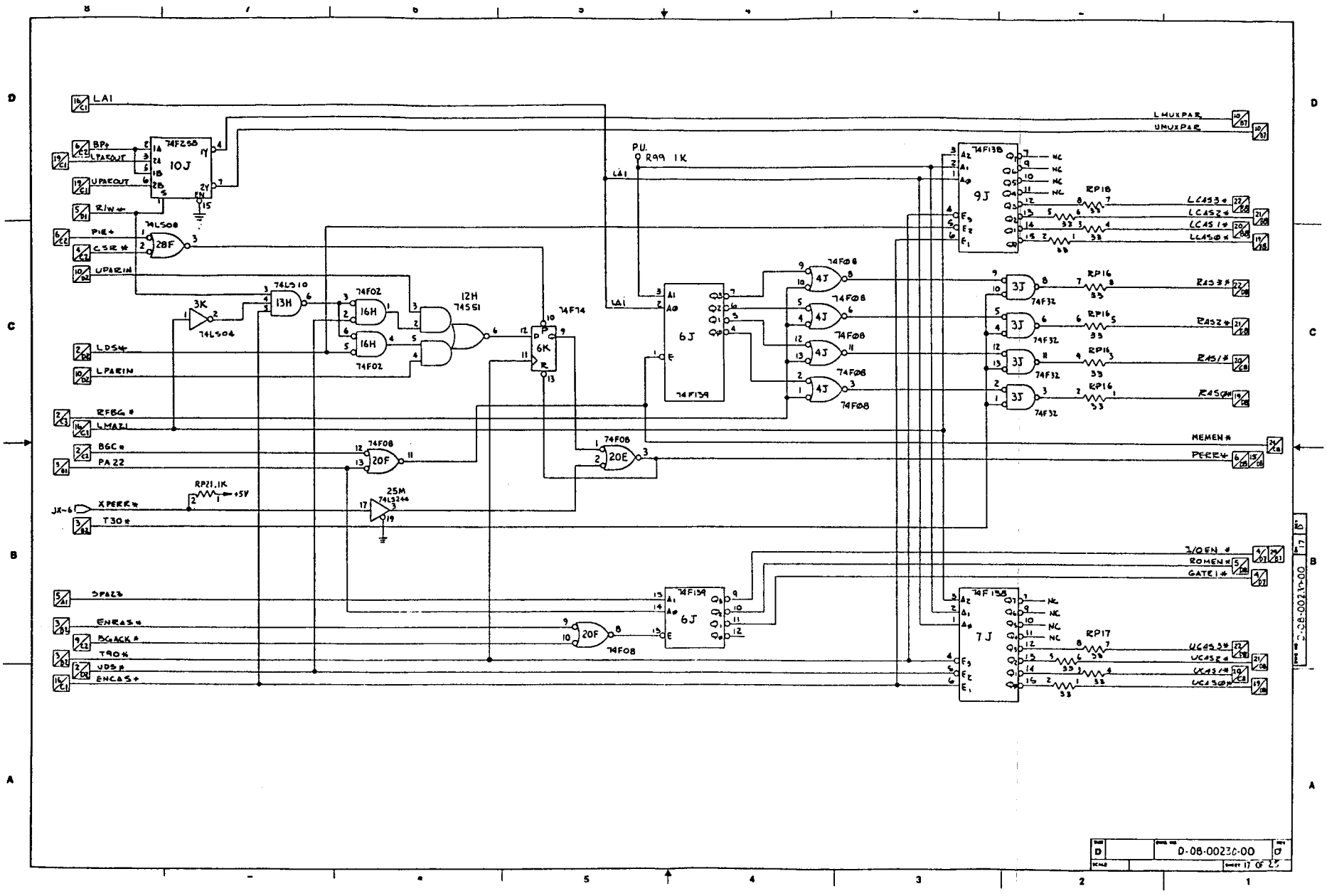

14M
DATA-SEP PAL
PAL16R4
14N
74S124/ LS629
13K
ZLL532
14K
74F153
16K
74F374
13M
74F10
15K
74F74
17M
74F74
16M
74F74
18M
74S03
13N
74123
17N
UF412
74F04
SONIC DELAY
HDRGATE
PCLK+
REF
VAR
FFA+
FFC+
EDA0
EDA1
JHZ-17
JHZ-18
ECLK
DRUN
DATA IN
LATE+
EARLY+
HDNDATA
IPLK+
WDG+
WDG-
JHZ-13
JHZ-14
JHZ-
2, 4, 6, 8, 10
11, 12, 15, 16
19, 20
AVCC
-12V
+5V
PU RP25-2 1M
PU RP25-3 1M
PU RP25-4 1M
PU RP25-5 1M
PU RP25-6 1M
PU RP25-8 1M
D-08-0023C-00
SHEET 12 OF 25

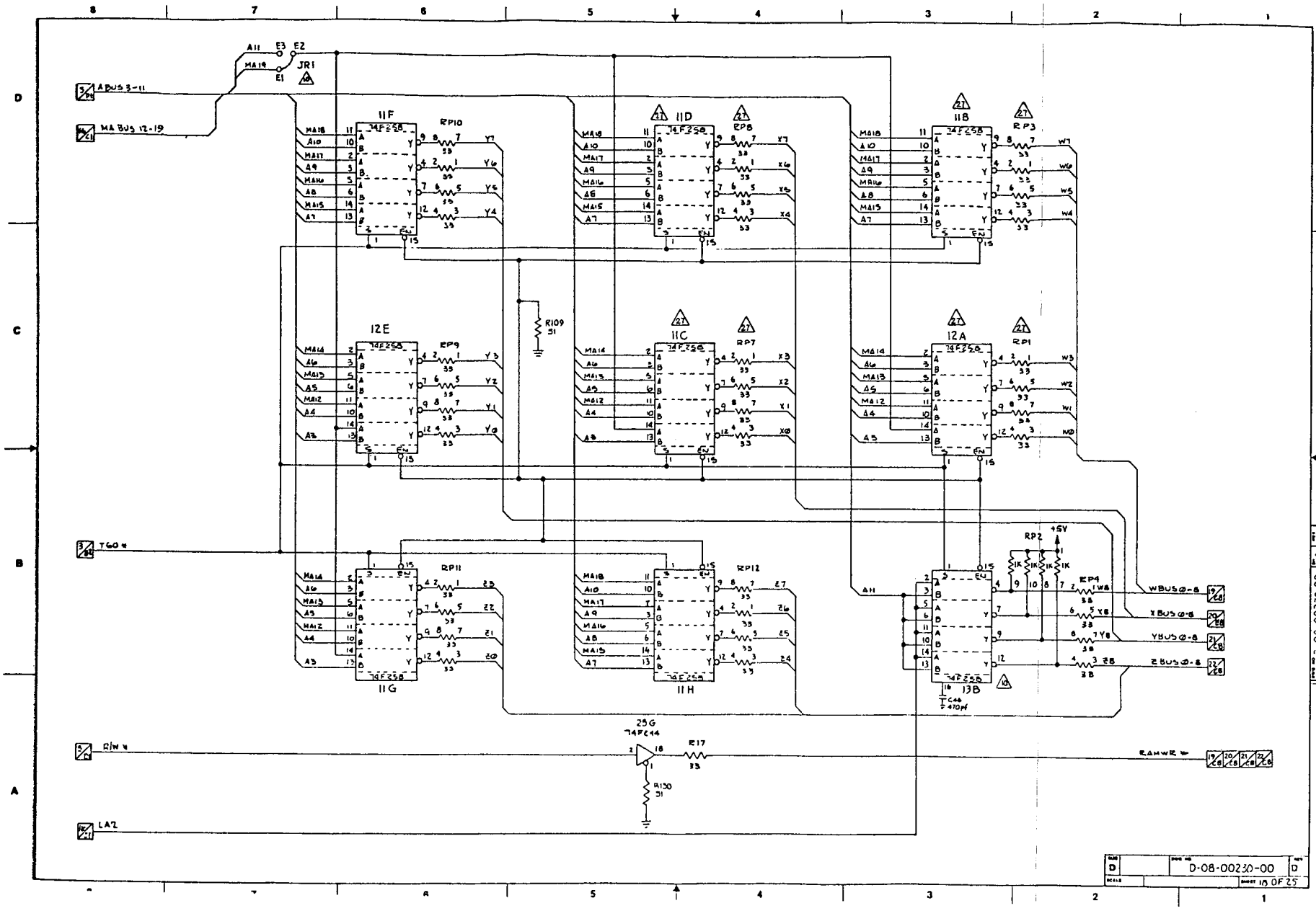

DD BUS 0-7
FDCS#
A BUS 1,2
FDRE#
FDWE#
FDEST#
1 MCK+
FDRD#
FDREADY#
FDTRACK0#
FDINDEX#
FDWPRT#
WD2797-02
22M
74LS126
74LS244
74LS14
74LS240
74LS290
RP23
220/330
R121 1K
R120 1K
R133
R134
C299
.22
C258
15-60pF
CR25,1N4148
R90,1M 1%
R128,51
R102 1K
R141 10K 20TURN
C237
C263
JR2
FDSTEP
FDDIR
FDWGATE
FDWDATA
FDINTRQ+
FDDRQ+
FDPRESENT#
FDMOTOR+
FDDRIVE0+
FDMOTOR#
FDDRIVE0#
XFDSTEP
XFDDIR
XFDWGATE
XFDWDATA
JF-30
JF-34
JF-26
JF-8
JF-28
JF-82
JF-81
JF-1
JF-16
JF-10
JF-20
JF-18
JF-24
JF-22
JF- 3,5,7,9,11 13,15,17,19 21,23,25,27 29, 33
D-08-00230-00
SHEET 13 OF 25

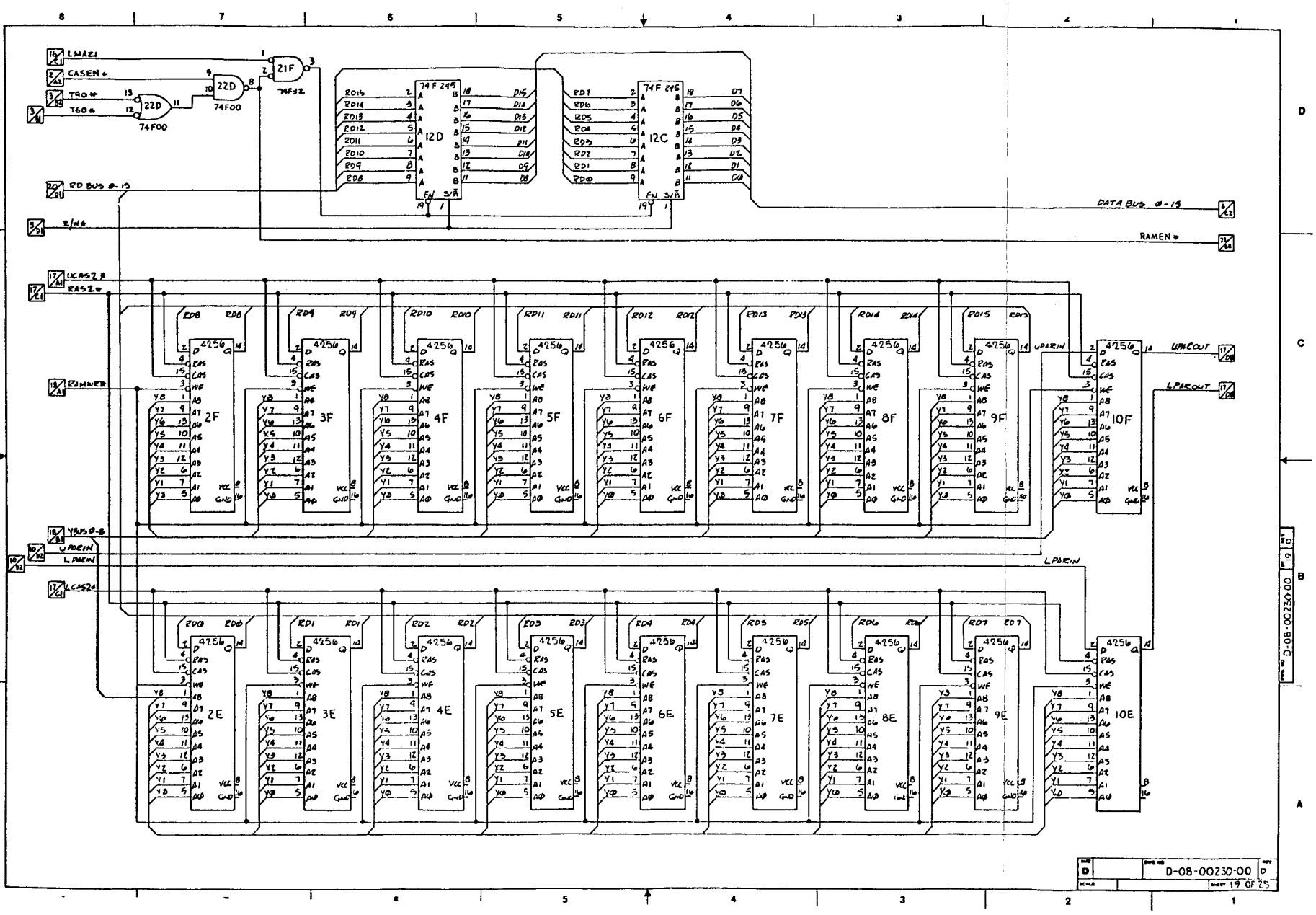

TPD BUS 0-7
ADDRESS BUS 1&2
RST*
2.45 MHZ
8274 CS*
RD*
WR*
RXD
CTS
CD
TXCK
RXCK
MODEM RXD
MODEM RXCK
MODEM TXCK
19.2 KBD
MODEM CK SEL*
TMOUT
DSR
EI
R/W*
PD BUS 8-15
PA1
KBEN
KBRXD
21M
7201
19M
19N
13G
6850
L2
BALUN
74LS14
74LS157
1489
CZ 1000pf
C284 100pf
C323 1000pF
C333 1000pF
C334 1000pF
C335 1000pF
R47 5K
R122 2.2K
RP26 1K
RP24 1K
R123,51
+5V
COMM INT*
DTR
RTS
TXDA
CLKOUT
MODEM TXD
KBINT*
KBTXD
KBEST*
JK-1
JK-20
JK-7
JK-4
JK-2
JK-24
JK-3
JK-5
JK-8
JK-15
JK-17
JK-6
JK-22
JK-1,2,3
JK-4,8
JK-5
D-08-00230-00
SHEET 14 OF 25

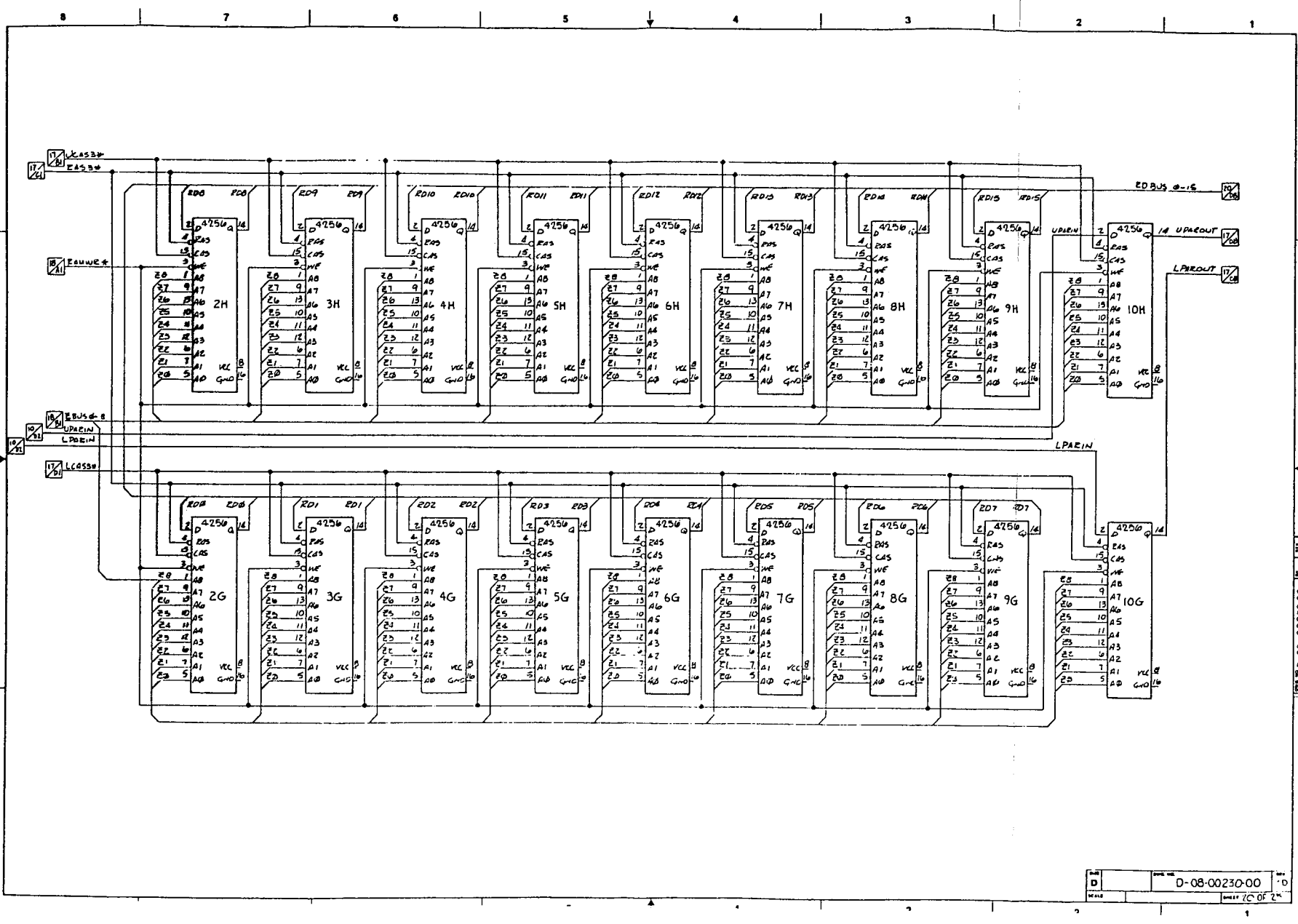

DATA BUS 0-15
RP26
1K
+5V
JP-11 LPBUSY+
JP-13 LPSELECT+
JP-12 LPNOPAPER+
JP-32 ERROR*
EQINTRQ+
HDINTRQ+
PERR*
DT DET*
CR31 IN5817
74LS244 15P
74LS374 16P
JP-17
JP-19-30 NC,33
PRD 8
PRD 7
PRD 6
PRD 5
PRD 4
PRD 3
PRD 2
PRD 1
JP-9
JP-8
JP-7
JP-6
JP-5
JP-4
JP-3
JP-2
JP-36
SLCT-INH
Q15 2N3906
R10 10K
CR1 3.9V IN4622
R93 100
RP25 1K 10
INIT*
JP-31
RP26 1K 10
AUTO FEED*
JP-14
LPINT+
LPDATAWR*
LPSTATUS RD*
JP-10 LPACK*
74LS240
LPSTROBE*
JP-1
74LS374
RP15-6,1K
74LS08
RTCCE+
RTCALE+
RTC R/W+
RTCD3
RTCD2
RTC D1
RTC D0
74LS273 27C
74LS244 26C
RTCRD*
RTCWR*
EST*
RTCCE+
R9 5.49K 1%
TC8250P 26D
RTC R/W+
RTC ALE+
RTC D0
RTC D1
RTC D2
RTC D3
C90 22pf
C88 47,6V
Y1 32.768MHZ
CR2 IN6263
CR3 IN6263
R11 1M
JR4
B1 3V
74LS374 27B
CLR 60HZ INT*
CMA R/W*
LPSTROBE+
MODEM CK SEL*
CR21
CR23
CR24
RP6,470
RP4,470
RP5,470
MREG WR*
D-08-00230-00
SHEET 15 OF 15

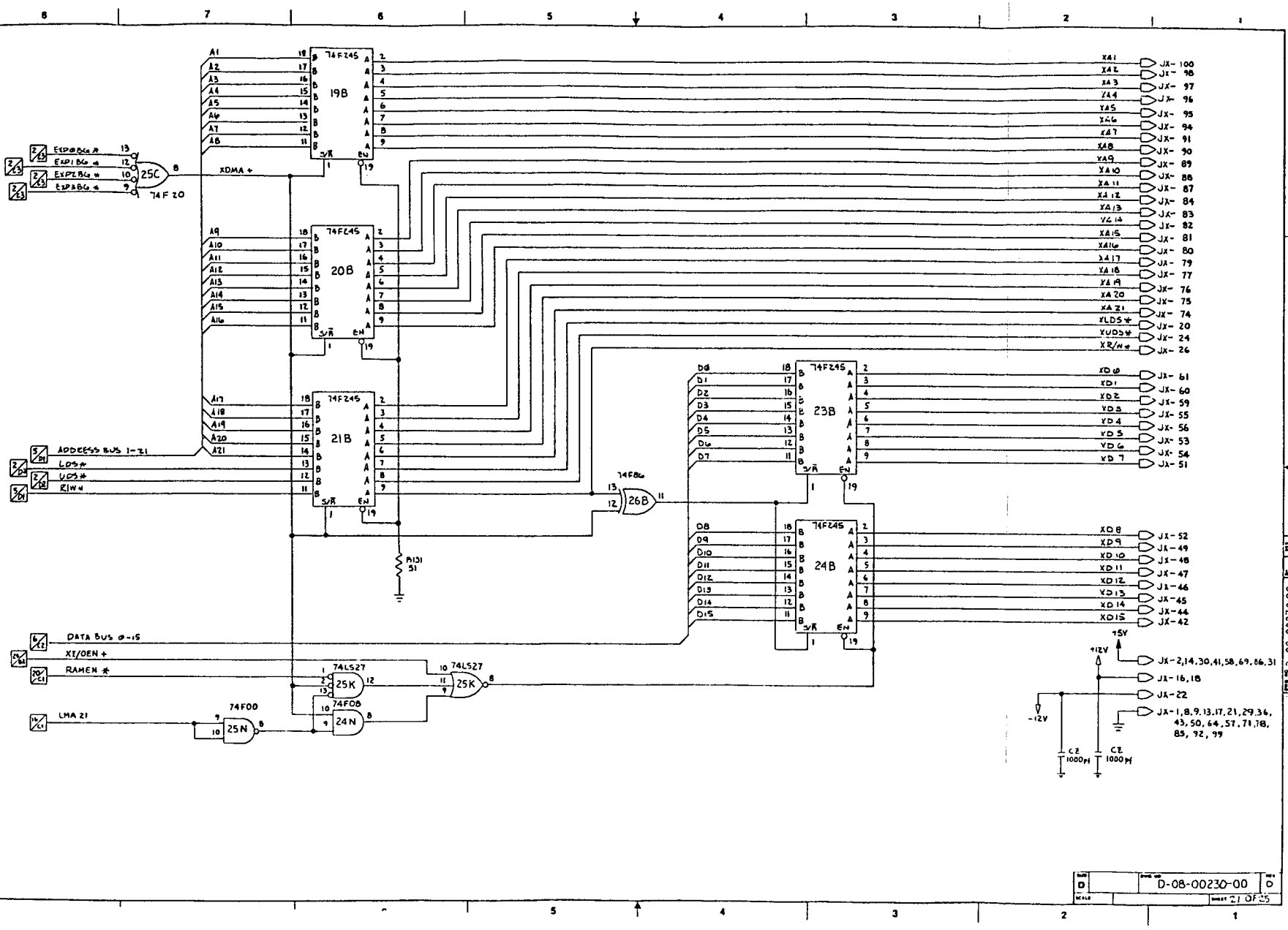

ADDRESS BUS 1-2, 12-21
PA BUS 1-18
DATA BUS 0-15
74F245
24C
74LS246
16G
2149
21C
22C
19C
20C
74F 373
25F
23C
74LS125
74F32
13E
26M
74F08
20E
25N
74F02
27H
74L527
25K
74F04
WE+
PS1
PS0
PS2
PS3
PS4
MA21
MA20
MA19
MA18
MA17
MA16
MA15
MA14
MA13
MA12
PA2
PA1
R123
51
R129
51
E/W*
PWE*
MEMWEN*
MMUWE*
T150*
CASEN+
CASDIS*
T120*
LMA20
LWE+
LPS1
LPS0
LMA21
LA2
ENCAS+
LA1
PS1
PS0
MA12-19
MA20
D-08-00230-00
16 OF 29

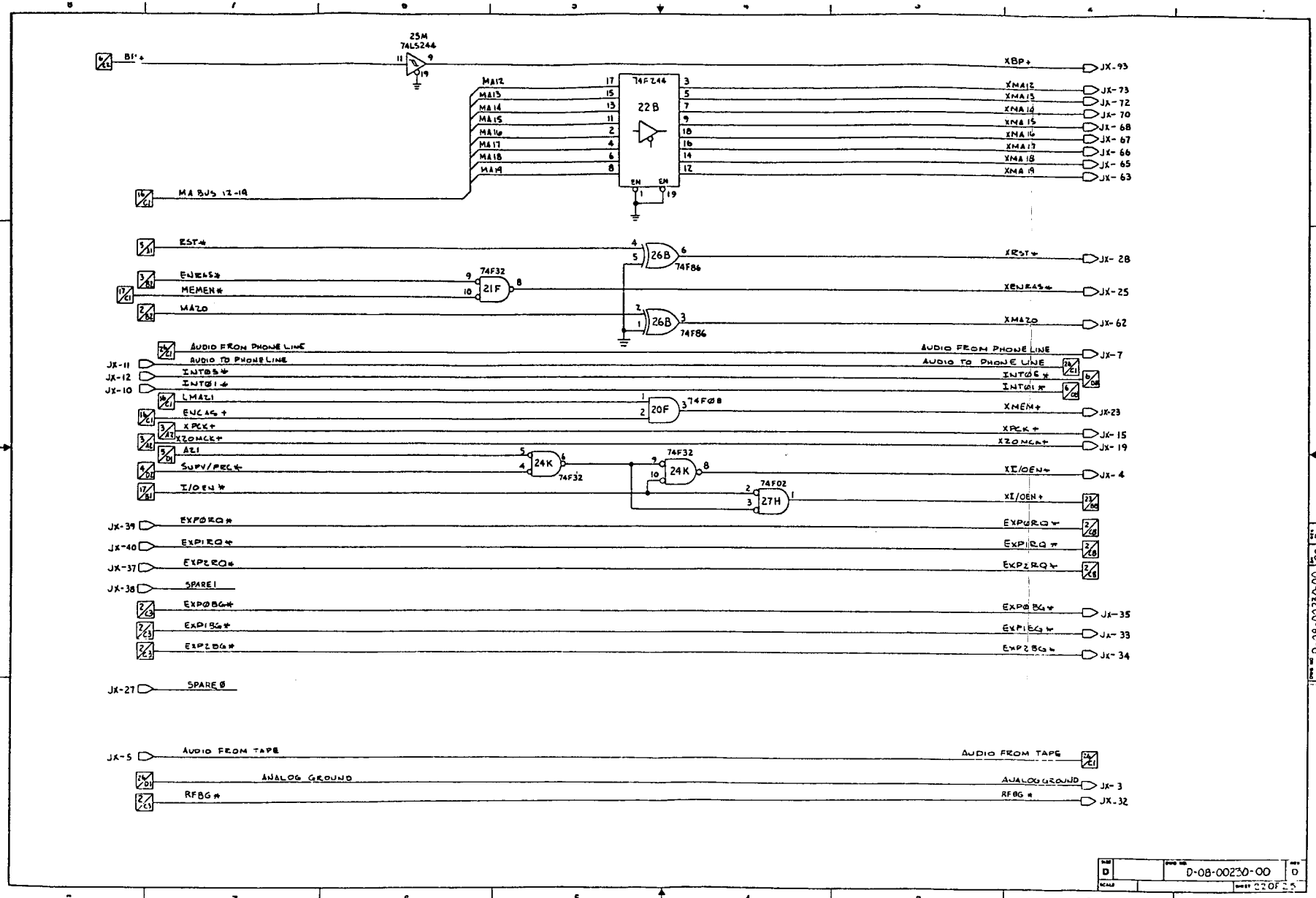

LAI
BP+
LPAROUT
UPAROUT
R/W+
PIE+
CSR*
UPARIN
LDS+
LPARIN
RFBG*
LMAZI
BGC*
PA22
XPERR*
T30*
SPAZ3
ENBAS*
BGACK*
T90*
UDS*
ENCAS*
74FZ50
10J
74LS08
28F
74LS10
13H
74LS04
3K
74F02
16H
12H
74S51
74F74
6K
P.U.
R99 1K
6J
74F139
74F08
4J
74F38
9J
74F32
3J
RP18
RP16
RP14
RP15
RP17
LCAS3*
LCAS2*
LCAS1*
LCAS0*
RAS3*
RAS2*
RAS1*
RAS0*
LMUXPAR
UMUXPAR
MEMEN*
PERR+
I/OEN*
ROMEN*
GATE1*
UCAS3*
UCAS2*
UCAS1*
UCAS0*
74F158
7J
RP21.1K
+5V
25M
74LS244
20F
20E
D-08-00230-00

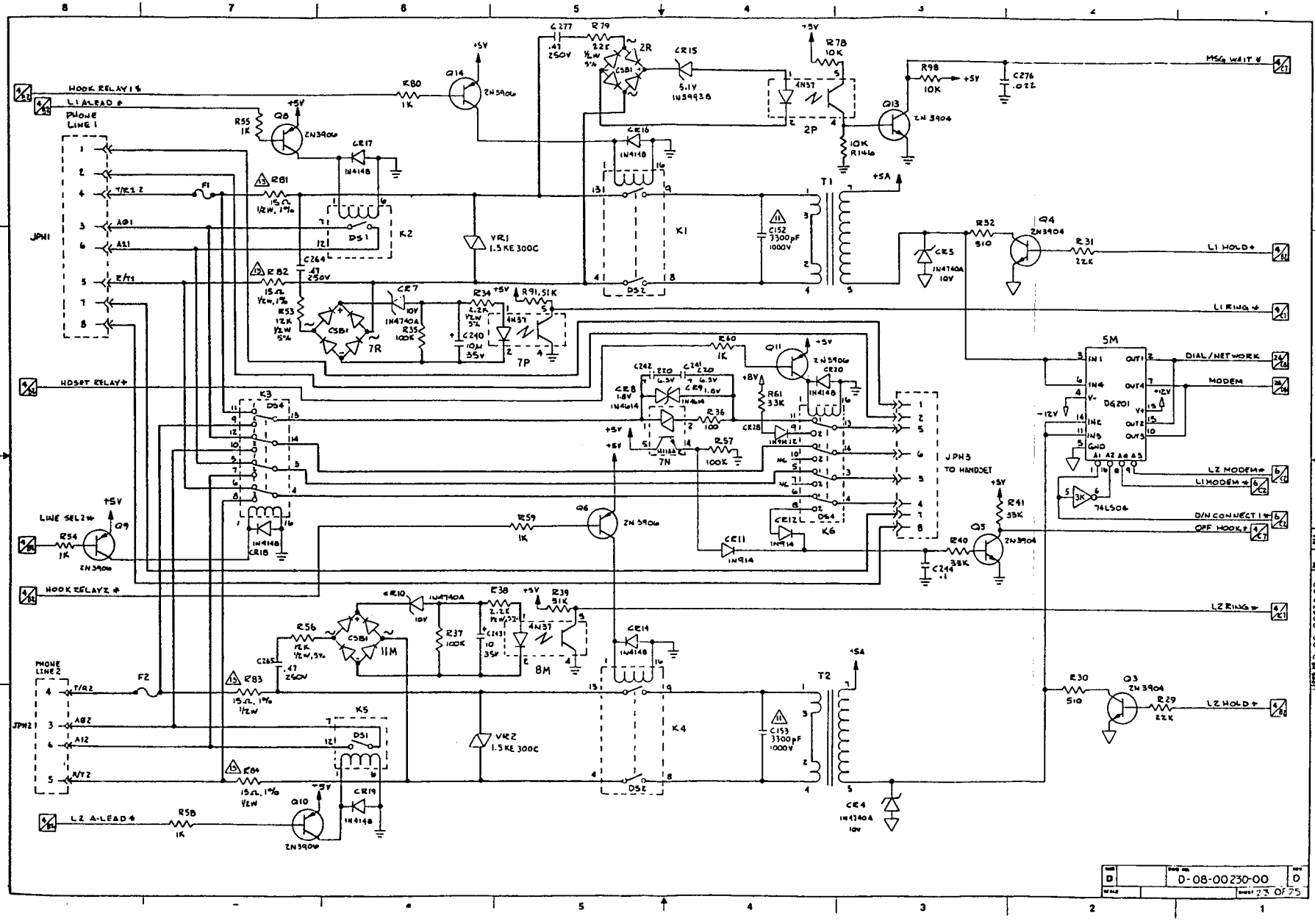

A11
E3
E2
MA19
JR1
E1
ABUS 3-11
MA BUS 12-19
11F
RP10
11D
RP8
11B
RP3
12E
RP9
R109
51
11C
RP7
12A
RP1
T60 N
11G
RP11
11H
RP12
13B
RP2
+5V
RP4
WBUS0-8
XBUS0-8
YBUS0-8
ZBUS0-8
25G
74FC44
R17
33
R130
51
R/W N
RAMWR N
LA7
C68
470PF
D-08-00230-00
SHEET 10 OF 25

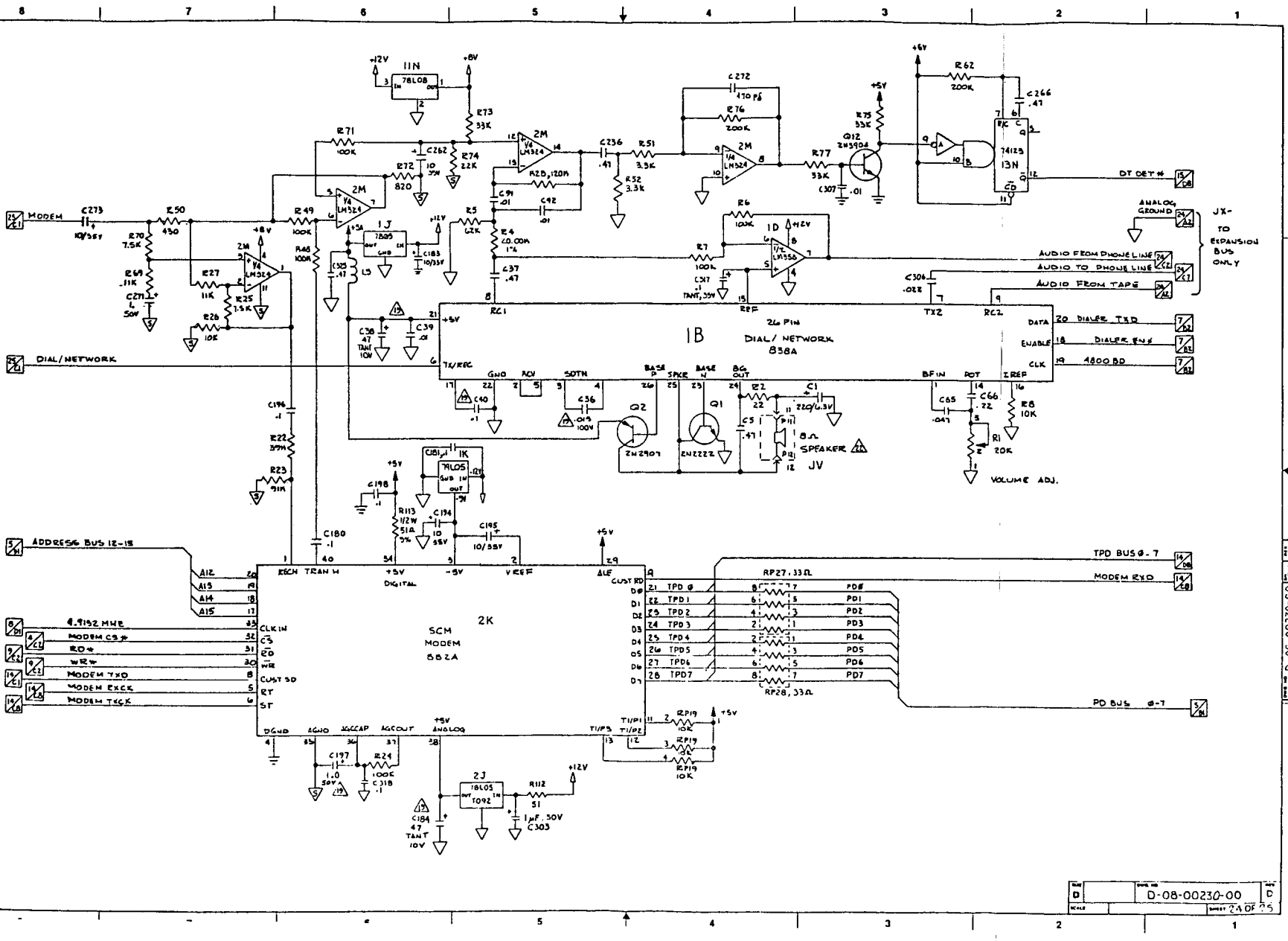

LMADI
CASEN*
T90*
T60*
21F
74F32
22D
74F00
74F 245
12D
12C
RD BUS 0-15
R/W*
DATA BUS 0-15
RAMEN*
UCAS2_3
RAS2*
RDB RDA RD9 RD8 RD11 RD10 RD13 RD12 RD15 RD14
2F 3F 4F 5F 6F 7F 8F 9F 10F
RAMWEB
YBUS 0-8
UPBEIN
LPBEIN
LCAS24
RD8 RD9 RD1 RD0 RD3 RD2 RD5 RD4 RD7 RD6
2E 3E 4E 5E 6E 7E 8E 9E 10E
UPBRIN
UPBROUT
LPBROUT
LPBRIN
D-08-00230-00
SHEET 19 OF 25


UCAS3#
LCAS3#
RAWE#
EBUS d-8
UPAEIN
LPAEIN
LCAS3#
ED BUS 0-15
UPAEOUT
LPAEOUT
UPAEIN
LPAEIN
2H
3H
4H
5H
6H
7H
8H
9H
10H
2G
3G
4G
5G
6G
7G
8G
9G
10G
4256
D-08-00230-00
SHEET 7C OF 24


74FZ245
19B
20B
21B
23B
24B
25C
74F20
26B
74F86
25K
74LS27
25N
74F00
24N
XDMA +
ADDRESS BUS 1-21
LDS*
UDS*
R/W*
DATA BUS 0-15
XT/OEN +
RAMEN *
LMA 21
RN31
51
+5V
+12V
-12V
C2
1000pf
D-08-00230-00
SHEET 21 OF 25


25M
74LS244
BP+
XBP+
JX-93
MA12
MA13
MA14
MA15
MA16
MA17
MA18
MA19
74F244
22B
XMA12
XMA13
XMA14
XMA15
XMA16
XMA17
XMA18
XMA19
JX-73
JX-72
JX-70
JX-68
JX-67
JX-66
JX-65
JX-63
MA BUS 12-19
RST*
XRST*
JX-28
ENEAS*
MEMEN*
74F32
21F
26B
74F86
XENEAS*
JX-25
MA20
XMA20
JX-62
AUDIO FROM PHONE LINE
AUDIO TO PHONE LINE
JX-7
JX-11
JX-12
JX-10
INT6S*
INT6I*
INT6S*
INT6I*
LMA21
ENCAS+
XPCK+
XZONCK+
A21
SUPV/PECK*
I/OEN*
20F
74F08
24K
74F32
27H
74F02
XMEM+
JX-23
XPCK+
JX-15
XZONCK+
JX-19
XI/OEN*
JX-4
XI/OEN+
EXP0RQ*
EXP1RQ*
EXP2RQ*
JX-39
JX-40
JX-37
JX-38
SPARE1
EXP0RQ*
EXP1RQ*
EXP2RQ*
EXP0BG*
EXP1BG*
EXP2BG*
JX-35
JX-33
JX-34
JX-27
SPARE0
AUDIO FROM TAPE
JX-5
ANALOG GROUND
RFBG*
AUDIO FROM TAPE
AUALOG GROUND
RFBG*
JX-3
JX-32
D-08-00230-00
D
SHEET 22 OF 25


HOOK RELAY 1 %
L1 A-LEAD #
PHONE LINE 1
JPN1
T/R1 2
A01
A11
R/T1
HOOK RELAY 2 %
LINE SEL 2 %
LZ A-LEAD #
PHONE LINE 2
JPN2
T/R2
A02
A12
R/T2
F1
F2
K1
K2
K3
K4
K5
K6
DS1
DS2
T1
T2
VR1 1.5KE 300C
VR2 1.5KE 300C
CR5 1N4740A 10V
CR4 1N4740A 10V
2R
7R
11M
8M
7P
8M
7N
2P
JPH3 TO HANDSET
5M
DG201
74LS04
MSG WAIT %
L1 HOLD #
L1 RING #
DIAL/NETWORK
MODEM
LZ MODEM #
L1 MODEM %
D/N CONNECT 1 %
OFF HOOK #
LZ RING %
LZ HOLD #
+5V
+8V
+5A
+12V
-12V
D-08-00230-00
SHEET 23 OF 25


MODEM
DIAL/NETWORK
ADDRESS6 BUS 12-15
4.9152 MHz
MODEM CS*
RD*
WR*
MODEM TXD
MODEM EXCK
MODEM TXCK
1B
DIAL/ NETWORK
836A
26 PIN
2K
SCM
MODEM
862A
SPEAKER
VOLUME ADJ.
AUDIO FROM PHONE LINE
AUDIO TO PHONE LINE
AUDIO FROM TAPE
ANALOG GROUND
TO EXPANSION BUS ONLY
DT DET H
DIALER TXD
DIALER ENA
4800 BD
TPD BUS 0-7
MODEM RXD
PD BUS 0-7
RP27, 33Ω
RP28, 33Ω
D-08-00230-00

I.C. VOLTAGE CHART

DEVICE	REFERENCE DESIGNATION	+5V	DGND	PAGE NO.
74F08	22D, 25N	14	7	2,4,5,16,20,23
74F02	16H, 27H	14	7	3,4,5,16,17,24
74S03	18M	14	7	12
74LS04	3M	14	7	3,5,6,17,23
74F04	13H	14	7	2,4,12,16
74F08	4J, 20E, 28F, 24N	14	7	2,7,16,17,23,24
74LS08	28D, 26F	14	7	3,4,5,6,11,15,17
74LS10	13H	14	7	5,17
74F10	15M	14	7	12
74F11	27F	14	7	2,4
74LS14	4M, 18M	14	7	4,5,11,13,14
74F20	29C	14	7	2,23
74LS27	23D, 25M, 26M	14	7	2,6,8,16,23
74F32	3J, 13E, 23F, 24M, 24P, 26M	14	7	2,3,4,5,7,9,11,16,17,20,24
74S31	12M, 19M	14	7	3,17
74F64	18G	14	7	3
74LS74	25H, 27M, 28M	16	8	2,6,7,8,11,15
74F74	6M, 15M, 26M, 17M	14	7	4,12,17
74F86	26D	14	7	8,23,24
74S112	21E, 28G	16	8	3
74123	13N	16	8	12, 26
74S124	14N	16	9	12
74LS138	26G, 27G, 28G	16	8	4
74F138	7J, 9J	16	8	17
74LS125	12F, 26M	16	8	5,11,13,16
74F139	6J	16	8	17
74F153	16M	16	8	12
74LS157	19M, 19N	16	8	14
74F175	18D, 18R	16	8	3,8
74LS240	17M, 24M	20	10	11,15,15
74LS244	9M, 15P, 16G, 24F, 25M, 26C	20	10	2,4,5,6,13,15,16,17,24
74F244	16F, 17P, 19G, 22B, 25G	20	10	2,3,5,13,18,24
74F245	12C, 12D, 13A, 13C, 13D, 17B, 19D, 28D, 21B, 23B, 23C, 24B, 24C	20	10	5,8,16,20,23
74F250	10J, 11B, 11C, 11D, 11F, 11G, 11H, 12A, 12E, 19F	16	8	3,17,18
74LS259	7M, 18M	16	8	4,6
74S260	21N	14	7	3
74LS273	17M, 27C	20	10	11,15
74S299	14B, 15B	14	7	8
74LS340	18F	16	8	6
74LS373	16D, 18C, 21D, 24P, 25D	20	10	6
74F373	17G, 25F	20	10	5,16
74F374	16M	20	10	2,3,6,12
74LS374	16P, 27D	20	10	15
74LS393	16E, 20D	14	7	7
74LS32	26F	14	7	4,5,8

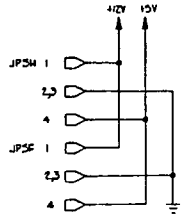
I.C. VOLTAGE CHART

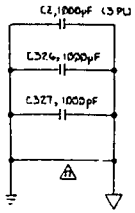
DEVICE	REFERENCE DESIGNATION	+5V	DGND	PAGE NO.
26LS31	14H	16	8	6,12
26LS32	13M	16	8	12
1488	23P Δ		7	14
1489	18P, 28P	14	7	14
2149	19C, 28C, 21C, 22C	18	9	16
2764/128	14C, 15C	28	14	5
6850	13G	12	1	14
4416	14A, 15A, 16A, 17A	5	18	8
4256	2E, 3E, 4E, 5E, 6E, 7E, 8E, 10E, 2F, 3F, 4F, 5F, 6F, 7F, 8F, 9F, 10F, 2G, 3G, 4G, 5G, 6G, 7G, 8G, 9G, K5G, 2H, 3H, 4H, 5H, 6H, 7H, 8H, 9H, 10H	8	16	19,20
6810	14E	14,19	6,23	5
6336	15			26
6822	2M			26
7201	21M	40	20	14
6581	2R, 7R, 11M			25
DG201	5M			25
HIIAAZ	7N			25
LM324	2M			26
LM339	1D			26
LF412	17N			12
4N37	2P, 7P, 8M			25
PAL16L8A	24G	20	10	2
PAL16R4	14M	20	10	12
PAL16M8A	24H	20	10	2
PAL16R8A	25D	20	10	2
TC8250F	26D	N/A	8	15
MD1010-35	21M	40	20	11
WD2797	22M	21	20	12
75L05	1A			26
1805	1J			26
75L05	11N			26
75L05	2J			26
VIDEO ARRAY	11C	30	20	7
DMA DATA ARRAY	22M	20	40	10
DMA ADDRESS ARR	22E	20	30	9

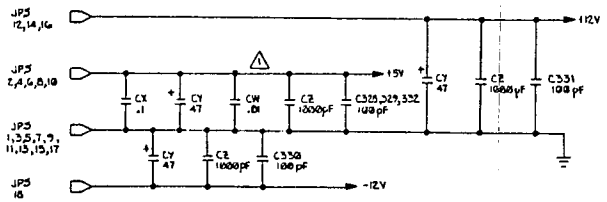
D-08-00230-00

NOTES: UNLESS OTHERWISE SPECIFIED

1. ON CAPS ARE USED NEAR I.C.'S WITH 18 MHZ.
2. PIN 14 SHOULD CONNECT TO +12V; PIN 1 TO -12V
3. THESE GATES MUST BE IN THE SAME PACKAGE. (PAGES 3, 16) (LAYOUT)
4. ALL OUTPUT TRACES ON 74LS259 SHOULD BE AS SHORT AS POSSIBLE. (LAYOUT)
5. SHOULD BE A SHORT TRACE AND NO HIGH FREQUENCY TRACE NEARBY. (LAYOUT)
6. STUFFING OPTIONS: WITH 74S124 - STUFF R94 (NOT R95). C300 SHOULD BE 27pF
   WITH 74LS629 - STUFF R95 (NOT R94). C300 SHOULD BE 56pF
7. MPS 4250 IS AN ALTERNATE PART.
8. THESE COMPONENTS ARE ONLY TO BE STUFFED WHEN USING CONTROLLERS OTHER THAN WD2797.
9. DELETED
10. INSERT ONLY FOR 256K RAM CHIPS. ALSO CUT TRACE BETWEEN E2 AND E3 AND ADD JA1 FROM E3 TO E2.
11. THESE CAPACITORS SHOULD BE LOCATED NEXT TO T1 AND T2. (LAYOUT)
12. HEAVY TRACE LINES INDICATE 25 MIL TRACES, 50 MIL AIR GAP. (LAYOUT)
13. ALL 15 Ω RESISTORS SHOULD BE FUSEABLE AND NON-FLAMMABLE.
14. ALL 1/2 W RESISTORS ARE TO BE NON-FLAMMABLE.
15. ⏚ INDICATES ANALOG GROUND.
16. ⏚ INDICATES DIGITAL GROUND.
17. DIGITAL AND ANALOG GROUND SHOULD ONLY BE CONNECTED AT SUPPLY ORIGIN. (LAYOUT)
18. ALL RELAYS ARE SHOWN AS DE-ACTIVATED.
19. CAPACITORS INDICATED SHOULD BE AS CLOSE TO I.C.'S AS POSSIBLE. (LAYOUT)
20. ⏚ INDICATES HAVING THE SHORTEST TRACE POSSIBLE BETWEEN THE COMPONENT AND ANALOG GROUND. (LAYOUT)
21. +12V AND -12V TO BE CONNECTED ONLY FROM SUPPLY ORIGIN. (LAYOUT)
22. SPEAKER MOUNTED ON MONITOR CASE.
23. ⏚ INDICATES CHASSIS GROUND.
24. ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.
25. ALL 1% RESISTORS ARE 1/4W.
26. CAPACITOR VALUES ARE IN MICROFARADS.







ZONE	REV	REVISIONS DESCRIPTION	DATE	CHK	APPROVED
	A	RELEASE TO CONTROL PER CO'S # 5095 & 5116			
	B	REVISED PER CO # 5118			
	C	REVISED PER CO # 5131			
	D	REVISED PER CO # 5153			
	E	REVISED PER CO # 5164 & 5165			
	F	REVISED PER CO # 5167			
	G	REVISED PER CO # 5166			
	H	REVISED PER CO # 5331			
	J	REVISED PER CO # 5494	6-13-86		

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C339	C1-39, 47-64, 67-87, 89, 93-109, 154-179, 182, 185-193, 199-235, 237, 238, 245, 247, 257, 259, 260, 261, 263, 274, 275, 278-283, 285-298, 300-302, 319-322, 324
CR20	
B1	
E3	E6, E7
F2	
H6	
L3	
Q19	
R146	R3, 18, 133-137, 111, 117, 125, 132-134
RP28	
SW1	
T2	
VR2	
Y1	
JP4	JP3

SPARE GATES		
DEVICE	REFERENCE DESIGNATION	QTY
26LS32	13A	1
74F10	13M	1
74F08	24N	3
74LS27	26N	2
74F244	25G	2
74S260	27N	1
74S112	21E	1
74S51	12H	1
74LS393	20D	1
74LS32	26F	2
LM 358	1D	1
1489	18P	1

INCHES

THIRD ANGLE PROJECTION

APPLICATION

DO NOT SCALE DRAWING

Convergent Technologies™

TITLE: SCHEMATIC: 54, CPU

RAMA 1-5-88

CHECKED BILL BLACK 1-9-88

ENGR. MGR. SAMUEL TAM 1-9-88

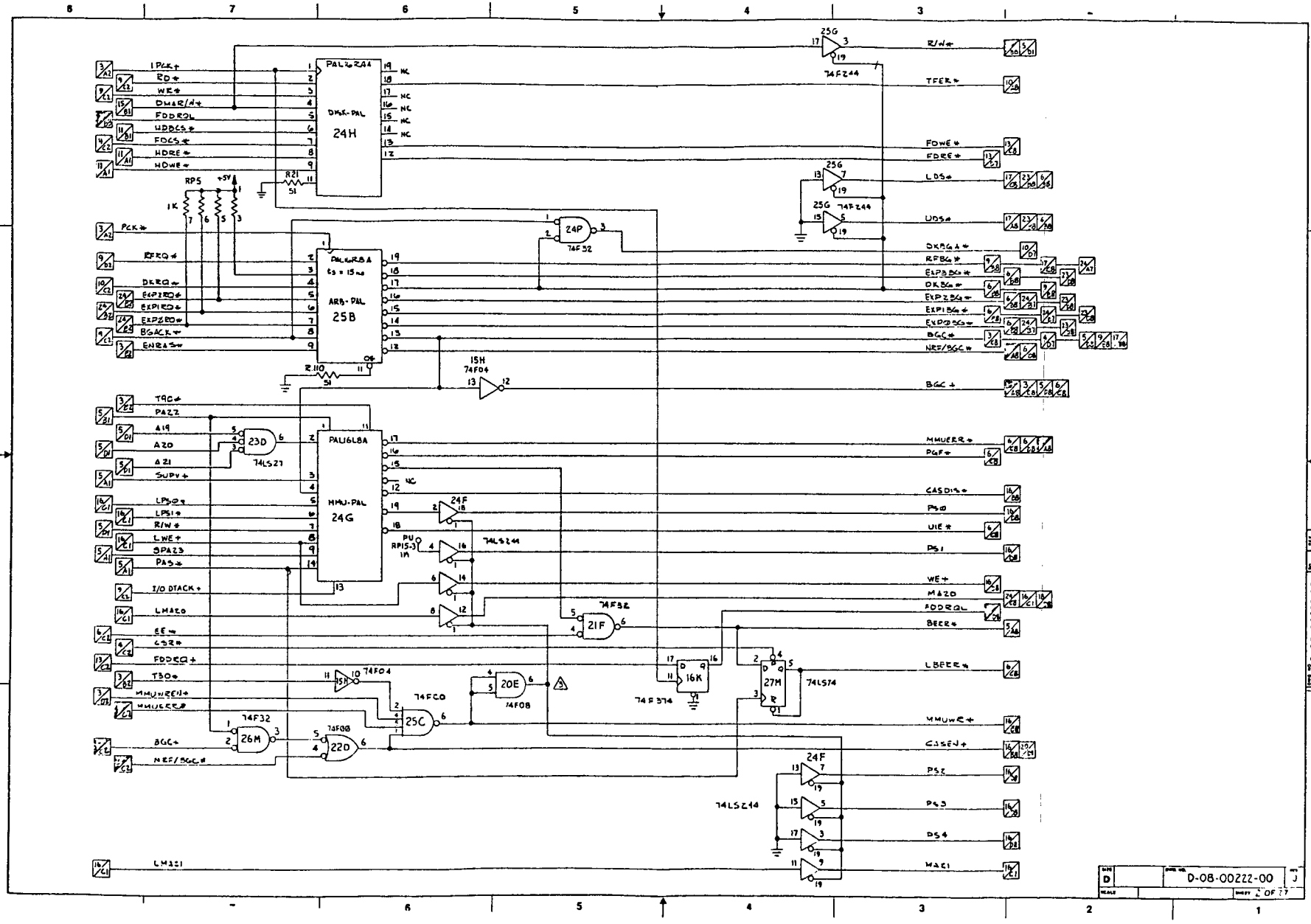
SIZE D

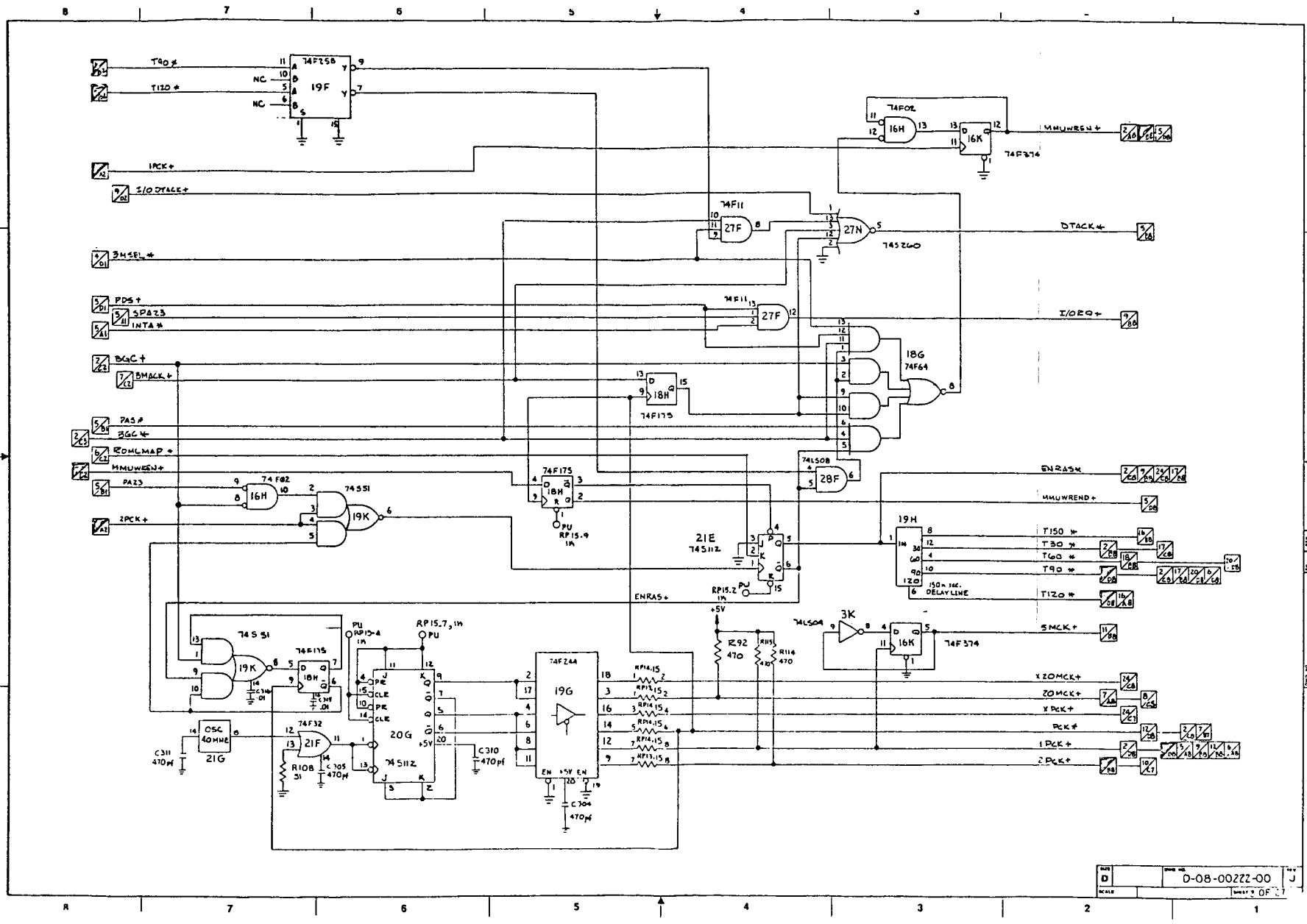
DWG NO. D-08-00222-00

REV J

SHEET 1 OF 21

D-08-00222-00 REV J


DISK-PAL
24H
ARB-PAL
25B
MMU-PAL
24G
74F244
74LS27
74F32
74F04
74F08
74F374
74LS574
74LS244
IPCK+
RD+
WE+
DMAR/W+
FDDREQL
UDDCS+
FDCS+
HDRE+
HDWE+
PCK+
RFRQ+
DKREQ+
EXPZERO+
EXPIRED+
EXPZERO+
BGACK+
ENABLE+
T90+
PAZZ
A19
A20
A21
SUPV+
LPS0+
LPS1+
R/W+
LWE+
SPAZ3
PAS+
I/O DTACK+
LMA20
EE+
CS2+
FDDEQ+
T30+
MMUHEN+
MMUERR+
BGC+
REF/BGC+
LMA21
R/W+
TFER+
FDWE+
FDRE+
LDS+
UDS+
DKBGA+
RFBG+
EXPZBG+
DKBG+
EXPZBG+
EXPIBG+
EXPDBG+
BGC+
REF/BGC+
BGC+
MMUERR+
PGF+
CASDIS+
PS0
UIE+
PS1
WE+
MA20
FDDEQL
BEER+
LBEER+
MMUWE+
CASEN+
PS2
PS3
PS4
MA21
D-08-00222-00
J
SHEET 2 OF 27


T90 *
T120 *
74F258
19F
NC
NC
1PCK+
I/O DTACK+
3HSEL*
PDS+
SPARE3
INTA*
BGC+
BMACK+
PAS*
BGC*
ROMLMAP+
MMUWEEN+
PAS3
2PCK+
74F02
16H
74S51
19K
74F175
18H
74F11
27F
27N
74S260
74F08
16K
74F374
MMUWREN+
DTACK*
I/OEQ*
18G
74F64
74LS08
28F
ENRAS*
MMUWREND+
74F175
18H
RP15.9
1M
PU
21E
74S112
RP15.7, 1M
RP15.2
1M
19H
T150 *
T30 *
T60 *
T90 *
T120 *
150n sec.
DELAY LINE
ENRAS+
+5V
3K
74LS04
R92
470
R115
470
R116
470
SMCK+
X20MCK+
20MCK+
XPCK+
PCK*
1PCK+
2PCK+
74F244
19G
RP14.15
RP13.15
RP14.15
RP14.15
RP14.15
RP13.15
74F32
21F
OSC
40MHE
21G
C311
470pf
R108
51
C305
470pf
20G
74S112
C310
470pf
C304
470pf
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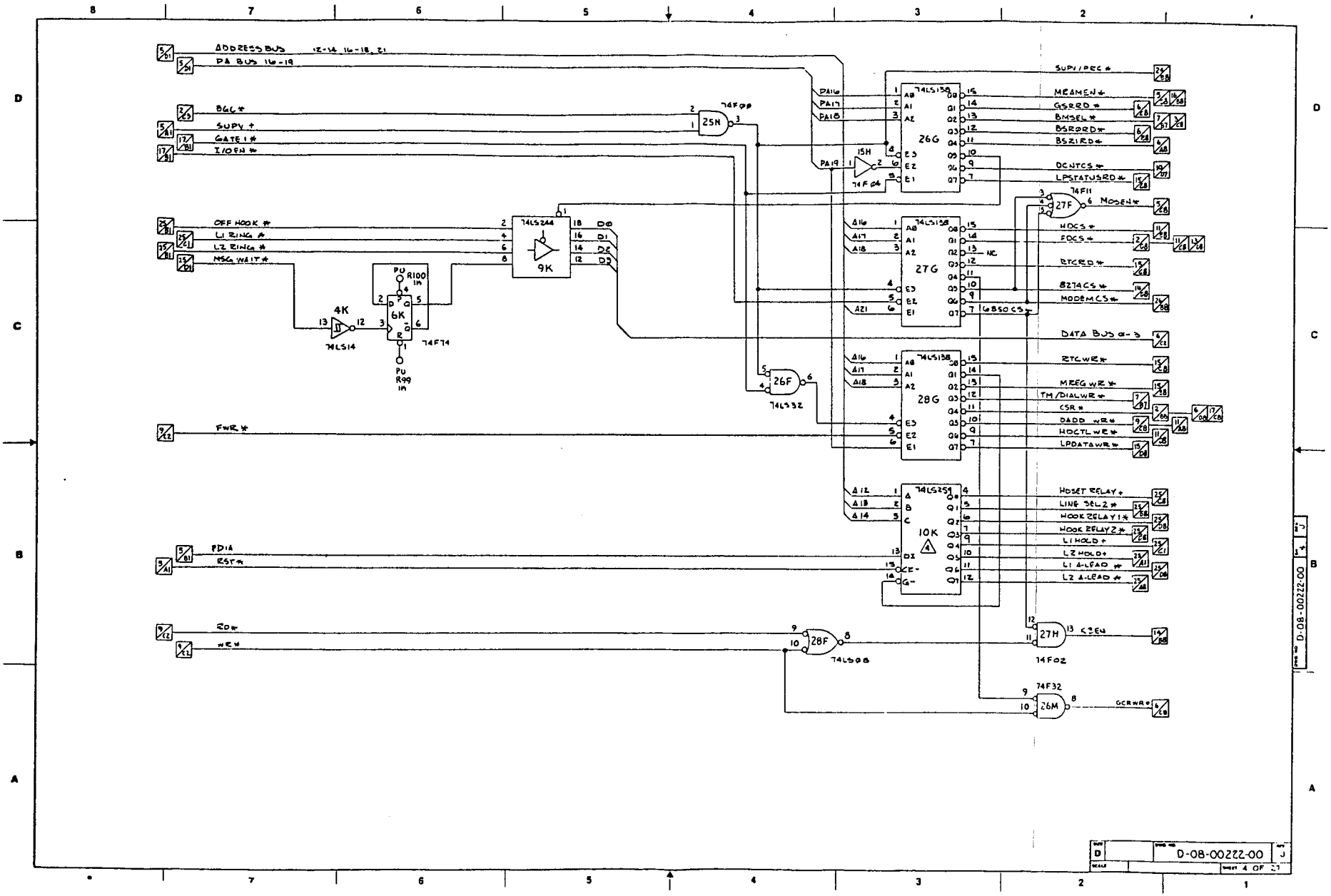
ADDRESS BUS 12-14 16-18, 21
PA BUS 16-19
BGL*
SUPV*
GATE1*
I/OEN*
OFF HOOK*
L1 RING*
L2 RING*
MSG WAIT*
FWR*
FDIA
RST*
RD*
WR*
74LS244
74LS14
74F74
74F08
74LS32
74LS08
74LS259
74F04
74F11
74F32
74F02
SUPV/PEC*
MEAMEN*
GSRRD*
BMSEL*
BSRDRD*
BSZIRD*
DCNTCS*
LPSTATUSRD*
MODEN*
HDCS*
FDCS*
BTCRD*
8274CS*
MODEMCS*
6850CS*
DATA BUS 0-3
RTCWR*
MREGWR*
TM/DIALWR*
CSR*
DADD WR*
HDCTLWR*
LPDATAWR*
HOSET RELAY*
LINE SEL 2*
HOOK RELAY 1*
HOOK RELAY 2*
L1 HOLD*
L2 HOLD*
L1 A-LEAD*
L2 A-LEAD*
CSEN
GCRWR*
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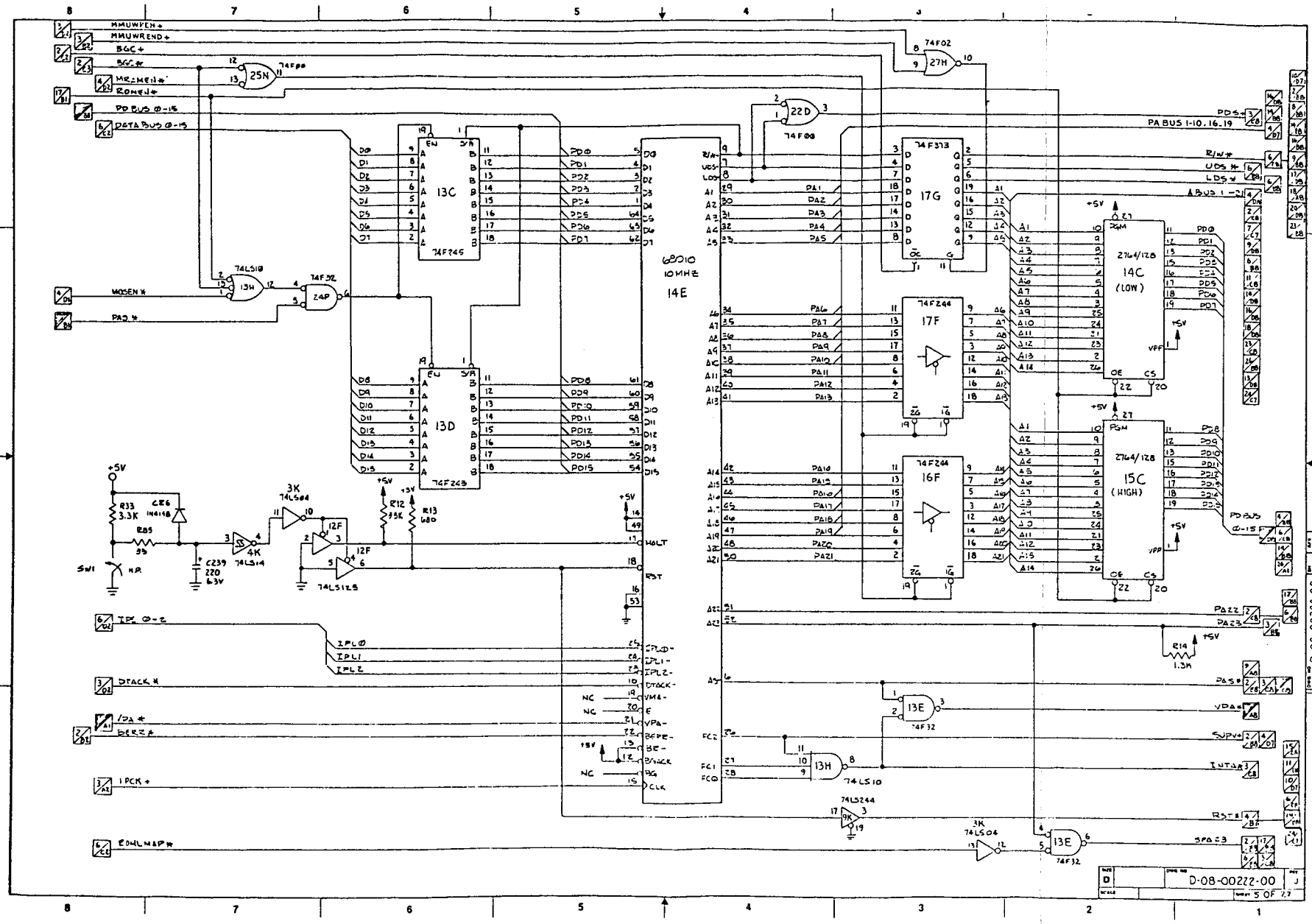
MMUWPEN*
MMUWREND*
BGC*
BGC*
MREMEN*
RONEN*
PD BUS 0-15
DATA BUS 0-15
25N
74F00
74F02
27H
22D
74F08
13C
74F245
13D
74F245
68010
10MHz
14E
74F373
17G
74F244
17F
74F244
16F
74LS10
13H
74F32
Z4P
74F32
13H
74LS10
MOSEN*
PA2*
+5V
R33
3.3K
CR6
IN4148
R35
39
SW1
N.P.
C239
220
63V
3K
74LS04
74LS14
4K
R12
R13
680
12F
74LS125
HALT
RST
IPL 0-2
IPL0
IPL1
IPL2
DTACK*
/DA*
BERR*
1 PCK*
BOOTMAP*
PA BUS 1-10, 16, 19
R/W*
UDS*
LDS*
ABUS 1-23
2764/128
14C
(LOW)
2764/128
15C
(HIGH)
PD BUS 0-15
PA22
PA23
R14
1.5K
PAS*
VPA*
SUPV*
INTAK*
RST*
SPACE
13E
74F32
74LS244
9K
3K
74LS04
13E
74F32
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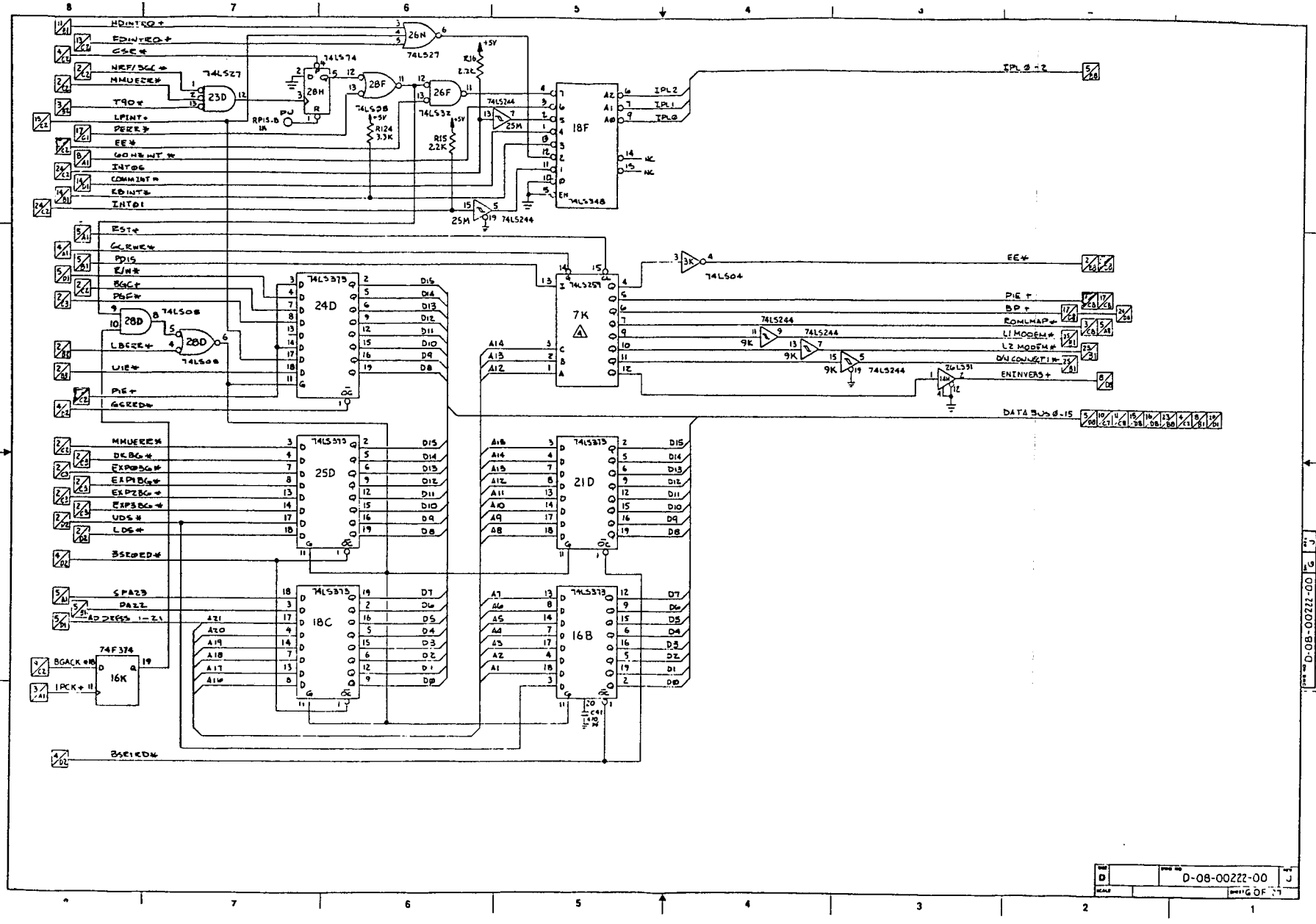
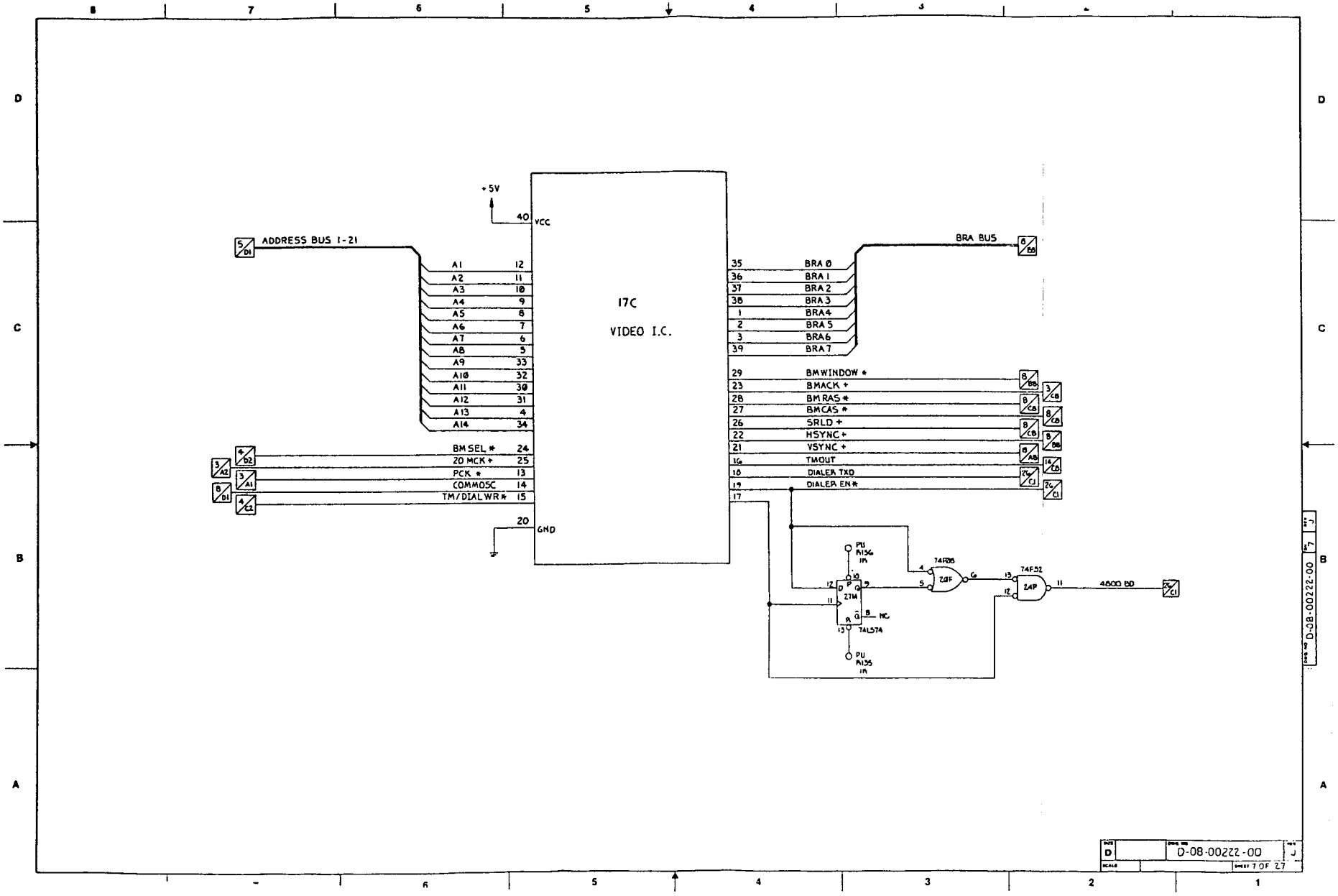
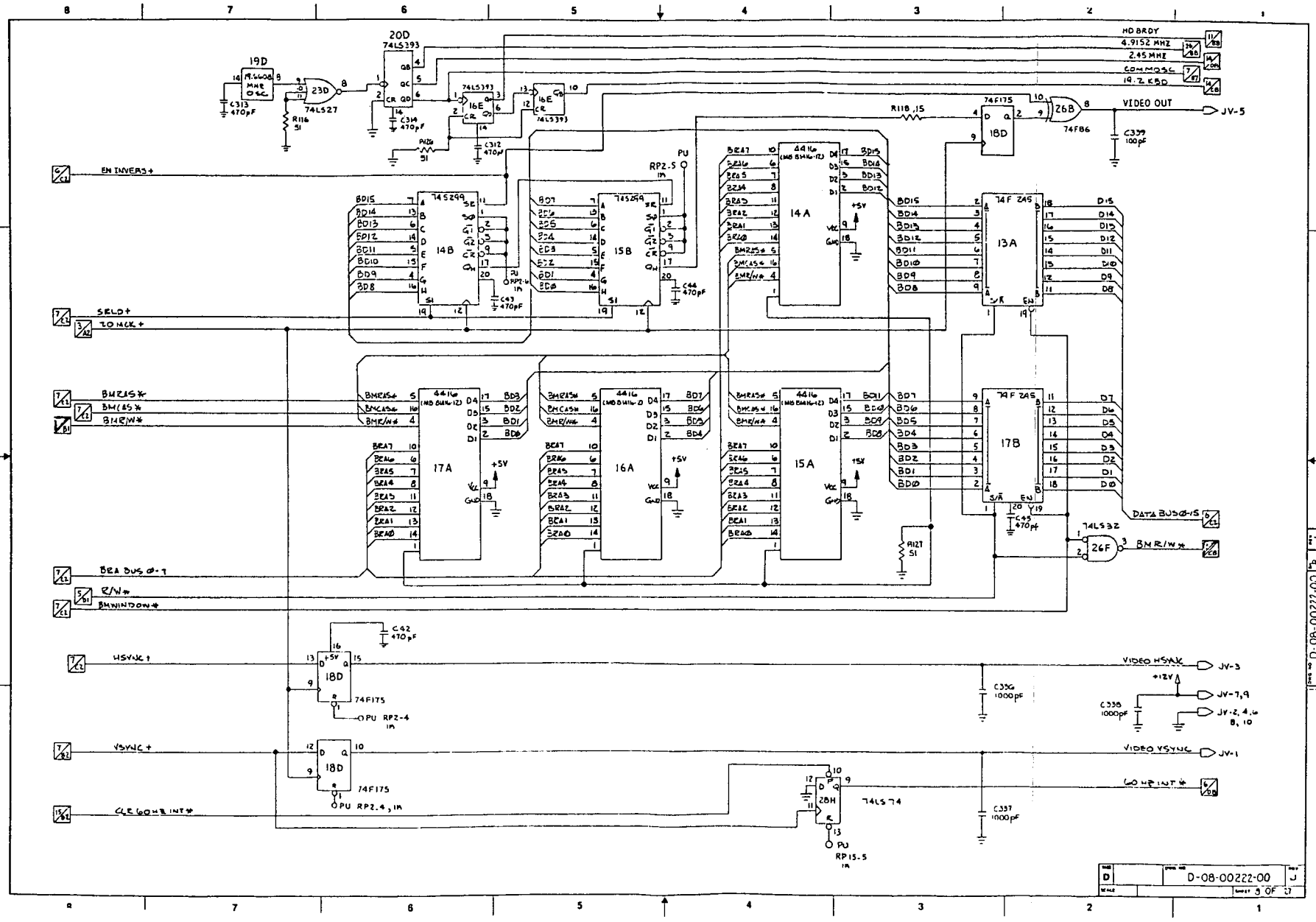

HDINTRQ+
EDINTRQ+
GSCK*
NREF/SCK*
MMUERR*
T90*
LPINT+
PERR*
EE*
GONENT*
INT06
COMMINT*
EDINT*
INT01
RST*
CLRME*
PDIS
R/W*
BGC*
PSF*
LBERR*
UIE*
PIE+
GCRED*
MMUERR*
DEBG*
EXP0BG*
EXP1BG*
EXP2BG*
EXP3BG*
UDS*
LDS*
BSERED*
SPAZ3
PAZZ
AD2ERR5 1-21
BGACK*
IPCK+
BSERED*
74LS27
74LS74
74LS08
74LS38
74LS244
74LS32
74LS348
74LS373
74LS259
74LS04
74LS51
74F374
23D
28H
28F
26F
26N
28D
18F
24D
25D
18C
7K
21D
16B
16K
IPL2
IPL1
IPL0
IPL 0-2
EE*
PIE+
BP+
ROMLMAP*
L1 MODEM*
L2 MODEM*
DAV CONJUCTION*
ENINVERS+
DATA BUS 0-15
D-08-00222-00


+5V
40 VCC
ADDRESS BUS 1-21
A1 12
A2 11
A3 10
A4 9
A5 8
A6 7
A7 6
A8 5
A9 33
A10 32
A11 30
A12 31
A13 4
A14 34
BM SEL * 24
20 MCK + 25
PCK * 13
COMMOSC 14
TM/DIAL WR * 15
20 GND
17C
VIDEO I.C.
35 BRA 0
36 BRA 1
37 BRA 2
38 BRA 3
1 BRA 4
2 BRA 5
3 BRA 6
39 BRA 7
BRA BUS
29 BM WINDOW *
23 BM ACK +
28 BM RAS *
27 BM CAS *
26 SRLD +
22 HSYNC +
21 VSYNC +
16 TMOUT
18 DIALER TXD
19 DIALER EN *
17
74F08
74F32
74LS74
NC
4800 BD
D-08-00222-00
D
SHEET 7 OF 27


19D
20D
74LS393
74LS27
16E
74F175
18D
74FB6
26B
VIDEO OUT
JV-5
HD BRDY
4.9152 MHZ
2.45 MHZ
COMMOSC
19.2 KBD
EN INVERS+
PU
RP2-5
1M
14B
15B
14A
13A
74F 245
SELD+
TO HCK+
BMRAS*
BM CAS*
BMR/W*
17A
16A
15A
17B
DATA BUS 0-15
74LS32
26F
BMR/W*
BEA BUS 0-7
R/W*
BMWINDOW*
HSYNC+
VIDEO HSYNC
JV-3
+12V
JV-7,9
JV-2, 4, 6, 8, 10
VSYNC+
VIDEO VSYNC
JV-1
CLEGOHZINT*
GO HZ INT*
74LS74
28H
RP15-5
1M
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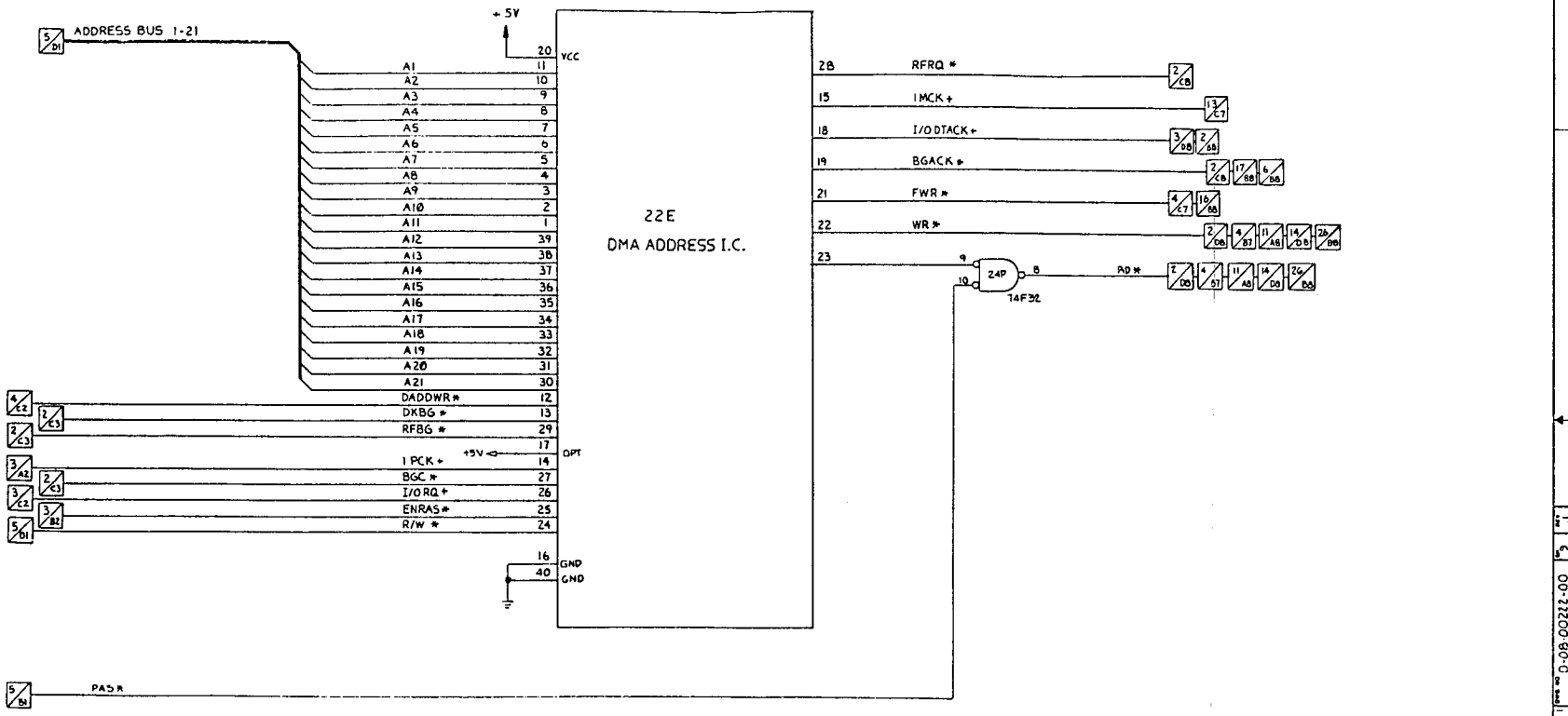
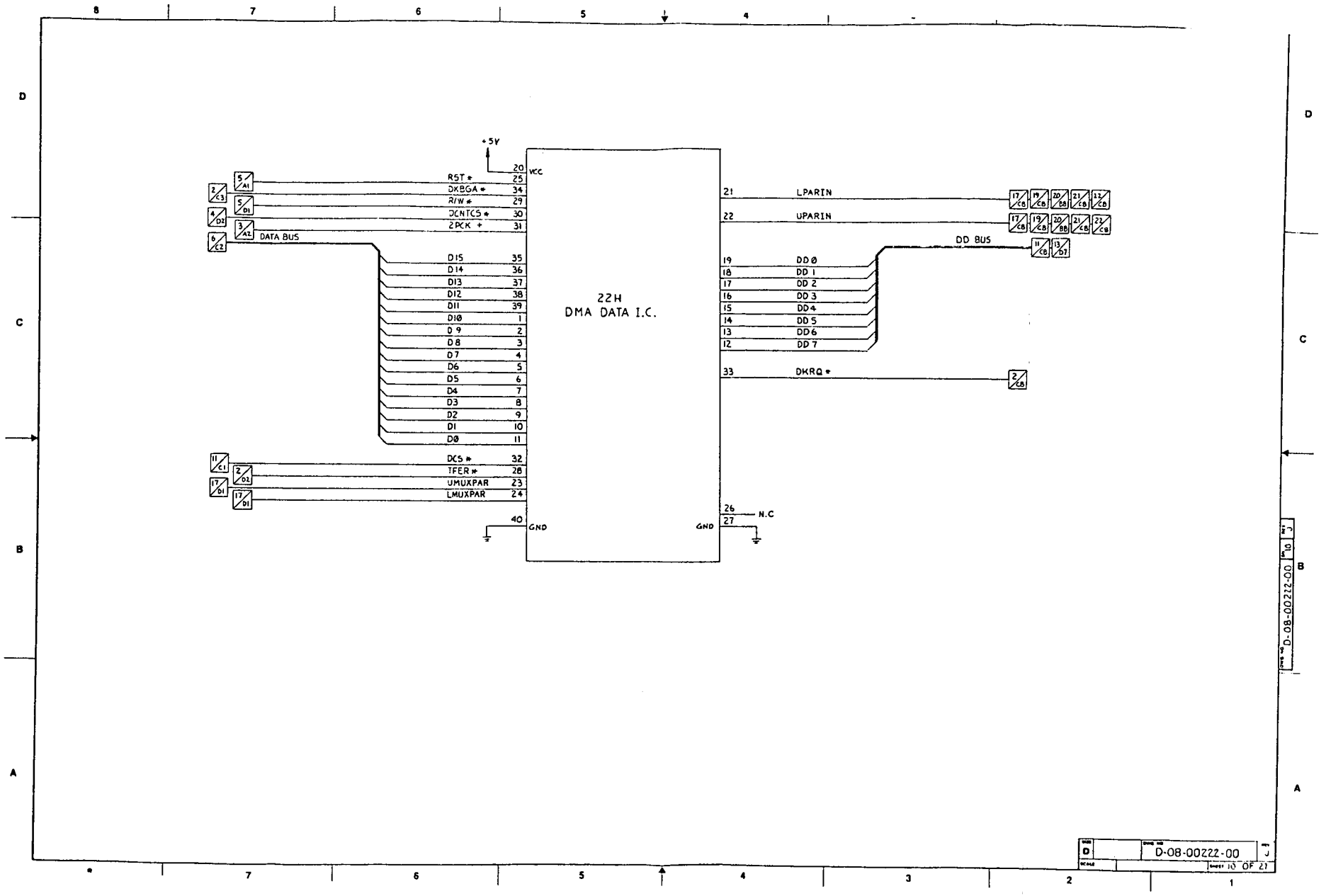

ADDRESS BUS 1-21
+5V
VCC
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
DADDWR*
DKBG *
RFBG *
+5V
OPT
IPCK +
BGC *
I/ORQ +
ENRAS*
R/W *
GND
GND
22E
DMA ADDRESS I.C.
RFRQ *
IMCK +
I/ODTACK +
BGACK *
FWR *
WR *
74F32
AD *
PAS *


+5V
VCC
20
22H
DMA DATA I.C.
RST *
DKBGA *
R/W *
DCNTCS *
2PCK +
DATA BUS
25
34
29
30
31
D15
D14
D13
D12
D11
D10
D 9
D 8
D 7
D6
D5
D4
D3
D2
D1
D0
35
36
37
38
39
1
2
3
4
5
6
7
8
9
10
11
DCS *
TFER *
UMUXPAR
LMUXPAR
32
28
23
24
40
GND
GND
27
26
N.C
21
LPARIN
22
UPARIN
DD BUS
19
DD 0
18
DD 1
17
DD 2
16
DD 3
15
DD4
14
DD 5
13
DD6
12
DD 7
33
DKRQ *
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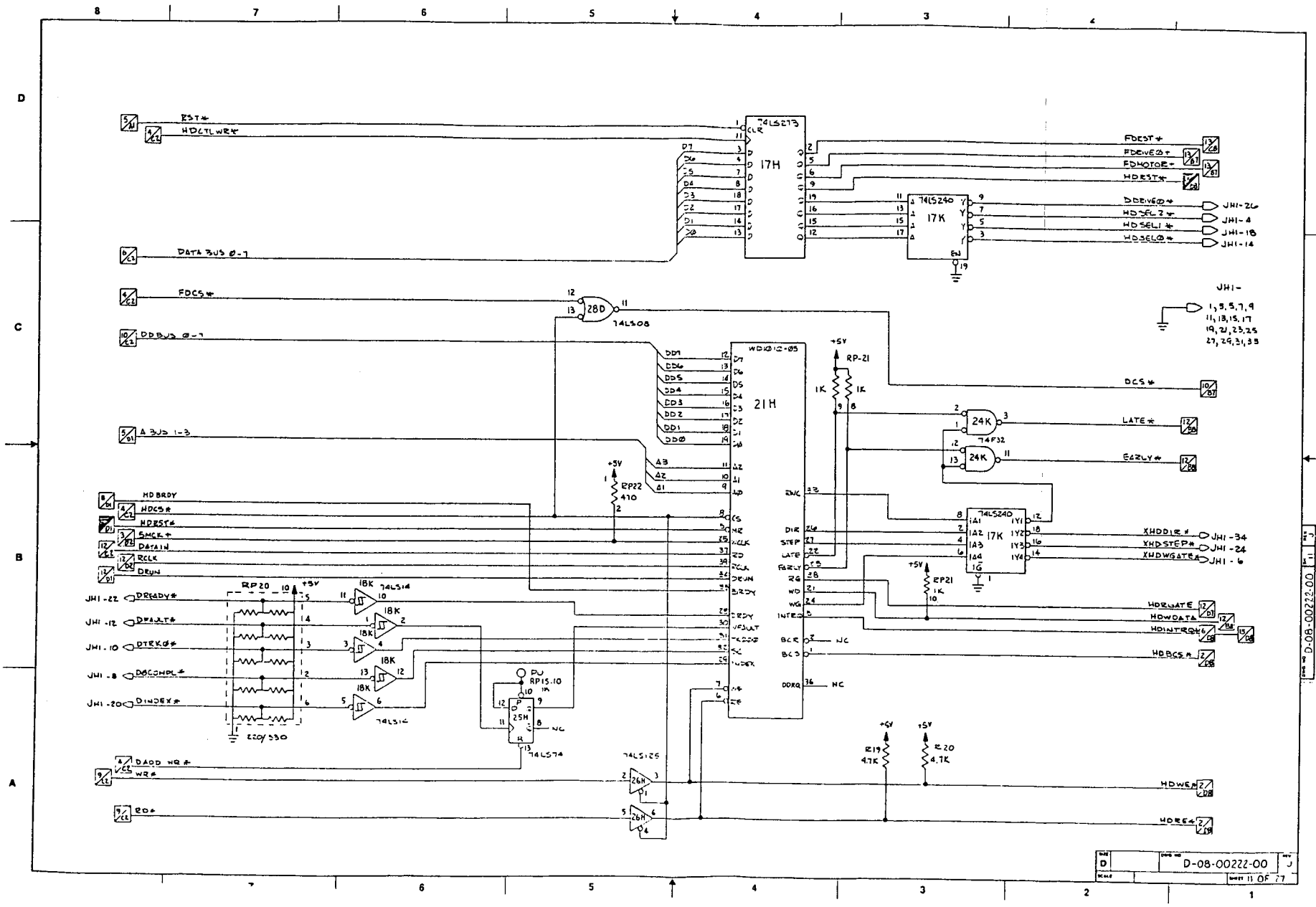
RST*
HDCTLWR*
DATA BUS 0-7
74LS273
17H
74LS240
17K
FDEST*
FDRIVE0*
FDMOTOR*
HDRST*
DDRIVE0*
HDSEL2*
HDSEL1*
HDSEL0*
JH1-26
JH1-4
JH1-18
JH1-14
FDCS*
DDBUS 0-7
A BUS 1-3
74LS08
WDC1C-05
21H
DCS*
LATE*
EARLY*
74F32
24K
RP-21
1K
74LS240
17K
XHDDIR*
XHDSTEP*
XHDWGATE*
JH1-34
JH1-24
JH1-6
HDBRDY
HDCS*
HDRST*
SMCK*
DATAIN
RCLK
DRUN
RP22
470
RP21
1K
HDRGATE
HDWDATA
HDINTRQ*
HDBCS*
JH1-22 DREADY*
JH1-12 DFAULT*
JH1-10 DTRK0*
JH1-8 DSCOMPL*
JH1-20 DINDEX*
RP20
330
18K
74LS14
PU
RP15-10
1K
25H
74LS74
74LS125
26H
DADD WR*
WR*
RD*
HDWE*
HDRE*
R19
4.7K
R20
4.7K
JH1-
1,3,5,7,9
11,13,15,17
19,21,23,25
27,29,31,33
D-08-00222-00
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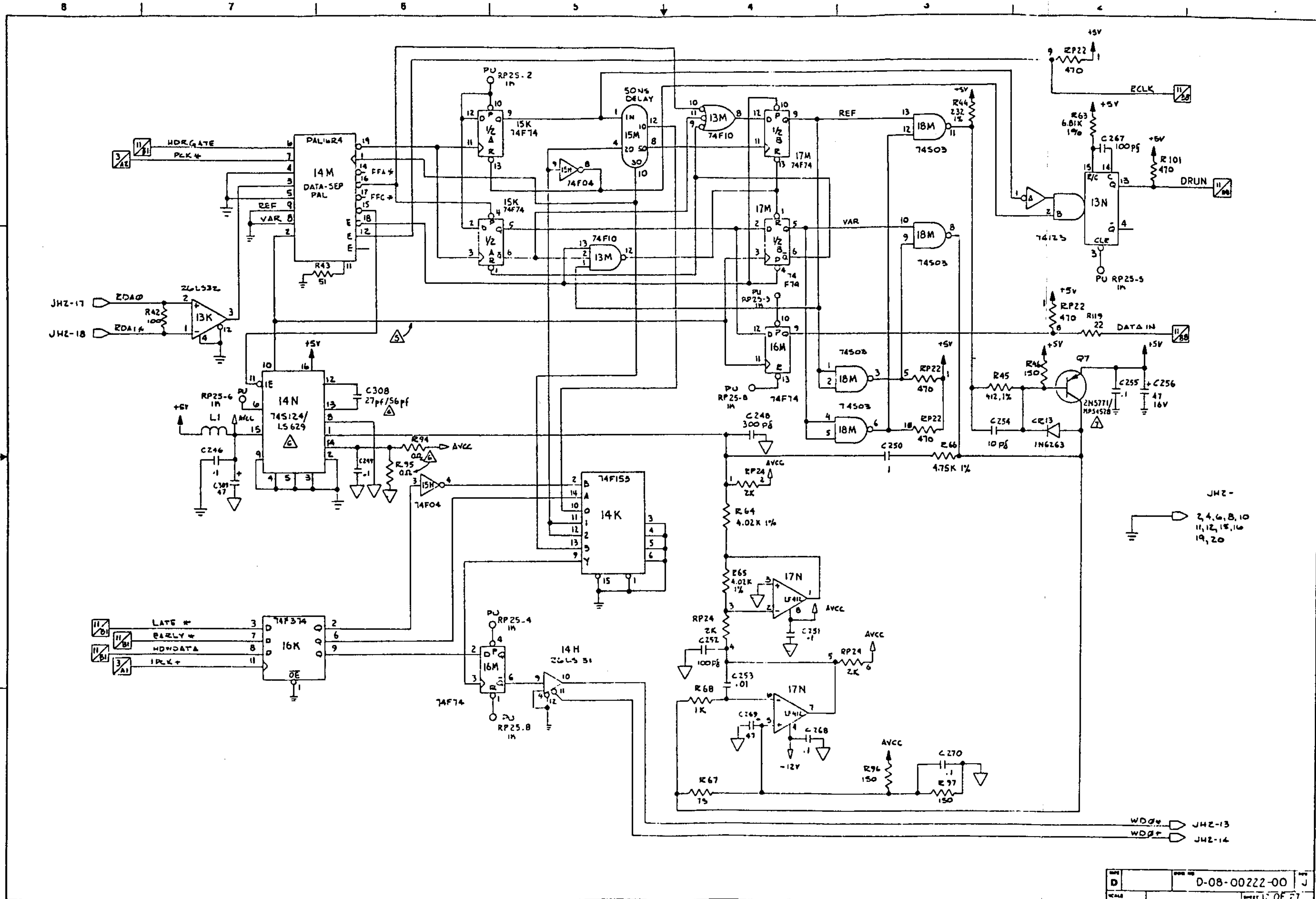

14M
DATA-SEP
PAL
PAL16R4
HDRGATE
PCK+
REF
VAR
FFA+
FFC+
R43
51
15K
74F74
15M
50NS
DELAY
74F04
13M
74F10
17M
74F74
18M
74S03
R44
232
1%
13N
74123
R63
6.81K
1%
C267
100pf
R101
470
DRUN
ECLK
RP22
470
PU RP25-5
RP25-2
JHZ-17
JHZ-18
RDA0
RDA1
R42
100
13K
26LS32
14N
74S124/
LS629
C308
27pf/56pf
L1
C246
C309
R94
R95
AVCC
15H
74F04
RP25-6
16M
74F74
RP25-8
RP25-3
DATA IN
R119
22
C248
300pf
C250
R66
4.75K 1%
R45
412, 1%
R46
150
Q7
2N5771/
MPS4528
C255
C256
47
16V
C254
10pf
CR13
1N6263
74F155
14K
RP24
2K
R64
4.02K 1%
R65
4.02K
1%
17N
LF412
C251
C252
100pf
C253
.01
R68
1K
C269
47
C268
-12V
R96
150
C270
R97
150
R67
75
74F374
16K
LATE +
EARLY +
HDWDATA
1PCK+
RP25-4
RP25.8
14H
26LS31
WDQ+
WDQ+
JHZ-13
JHZ-14
JHZ-
2,4,6,8,10
11,12,15,16
19,20
D-08-00222-00
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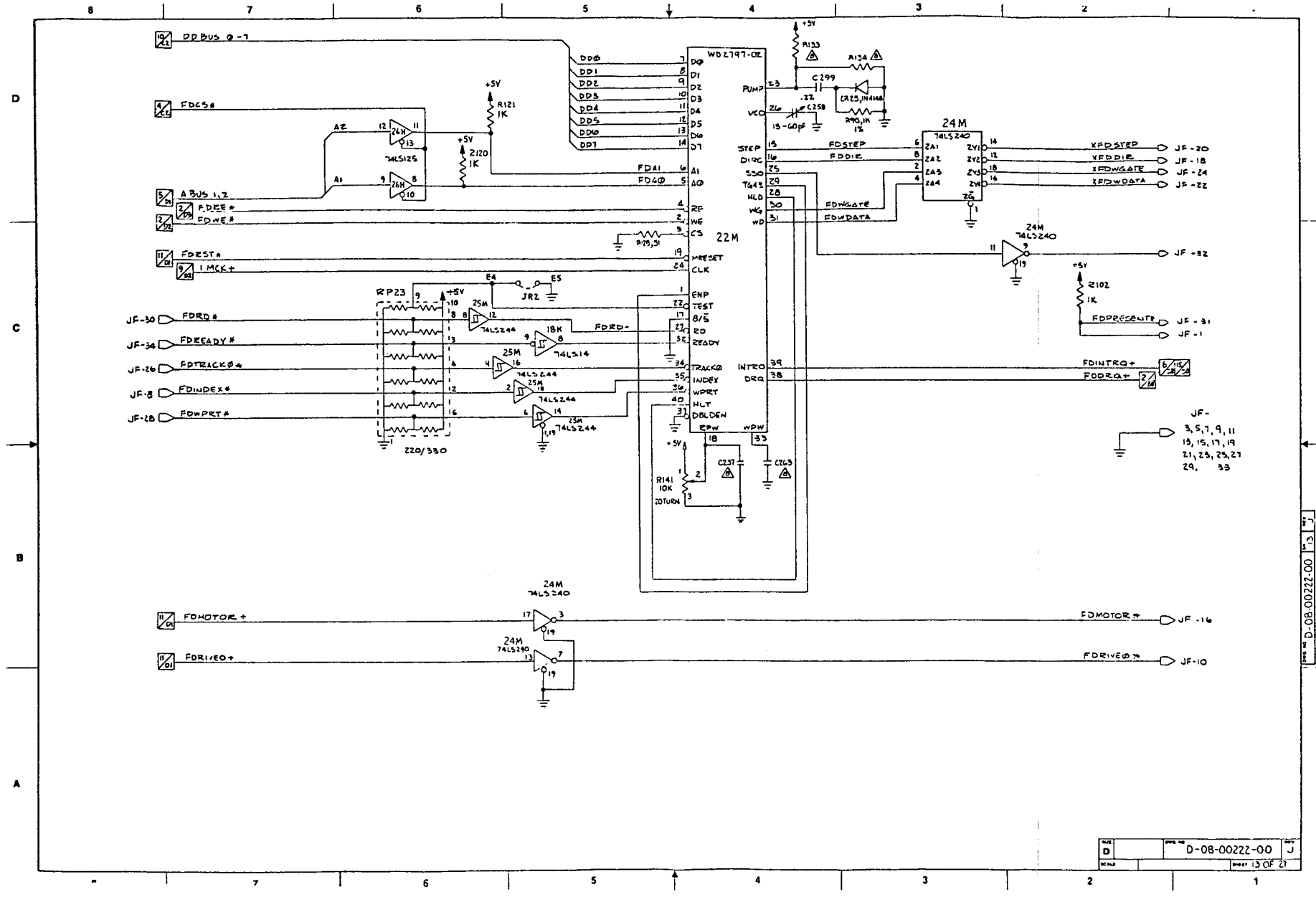

D-08-00222-00 J

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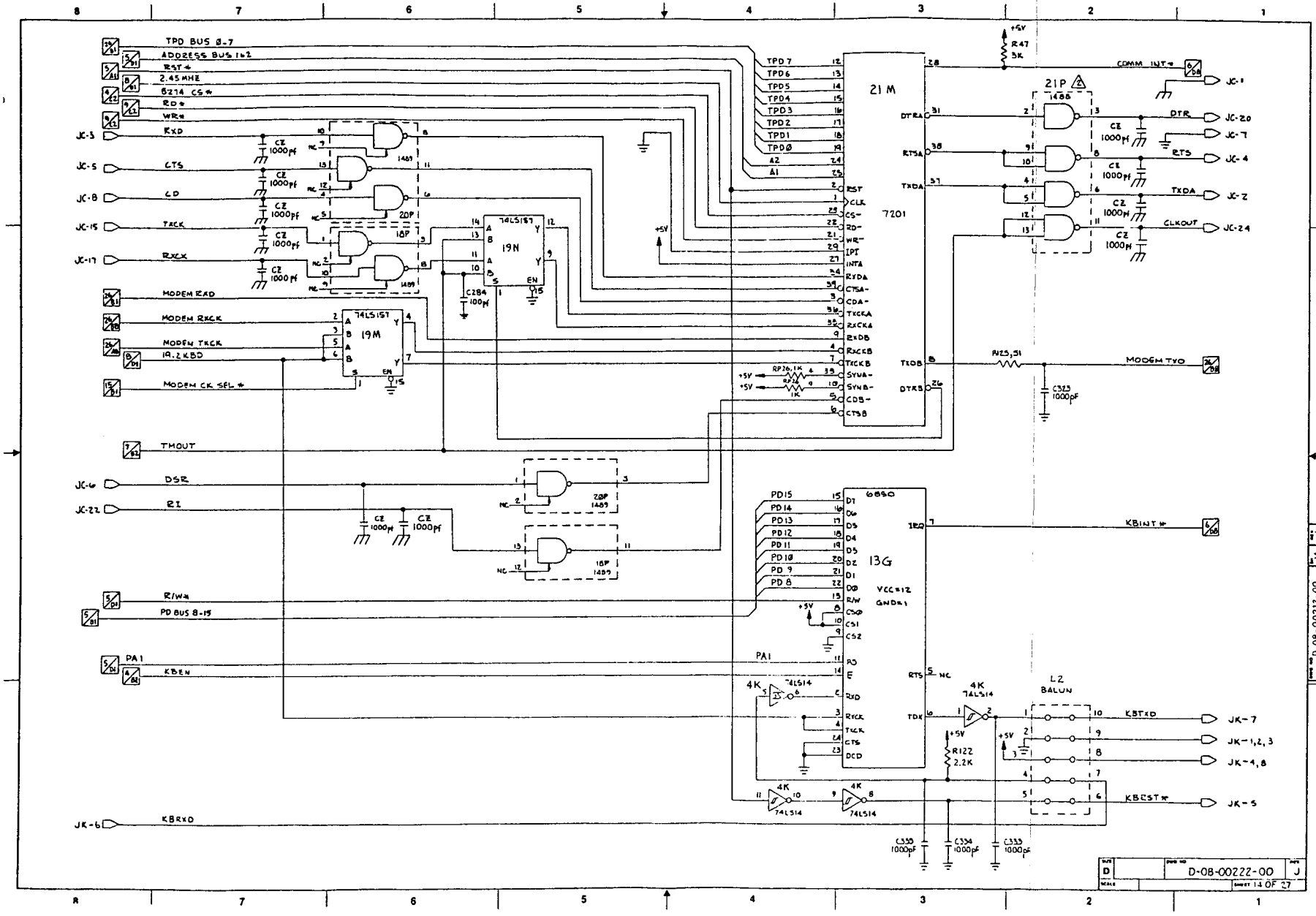
TPD BUS 0-7
ADDRESS BUS 1&2
RST*
2.45 MHZ
8214 CS*
RD*
WR*
RXD
CTS
CD
TACK
RXCK
MODEM RXD
MODEM RXCK
MODEM TXCK
19.2 KBD
MODEM CK SEL*
TMOUT
DSR
RI
R/W*
PD BUS 8-15
PA1
KBEN
KBRXD
21M
7201
19M
19N
13G
6850
21P
74LS157
74LS14
1489
1488
CZ 1000pf
C284 100pf
C323 1000pF
C335 1000pF
C334 1000pF
C333 1000pF
R47 3K
R122 2.2K
RP26 1K
RP24 1K
RP23,51
COMM INT*
DTR
RTS
TXDA
CLKOUT
MODEM TXD
KBINT*
KBTXD
KBRST*
L2 BALUN
JK-1
JK-20
JK-7
JK-4
JK-2
JK-24
JK-7
JK-1,2,3
JK-4,8
JK-5
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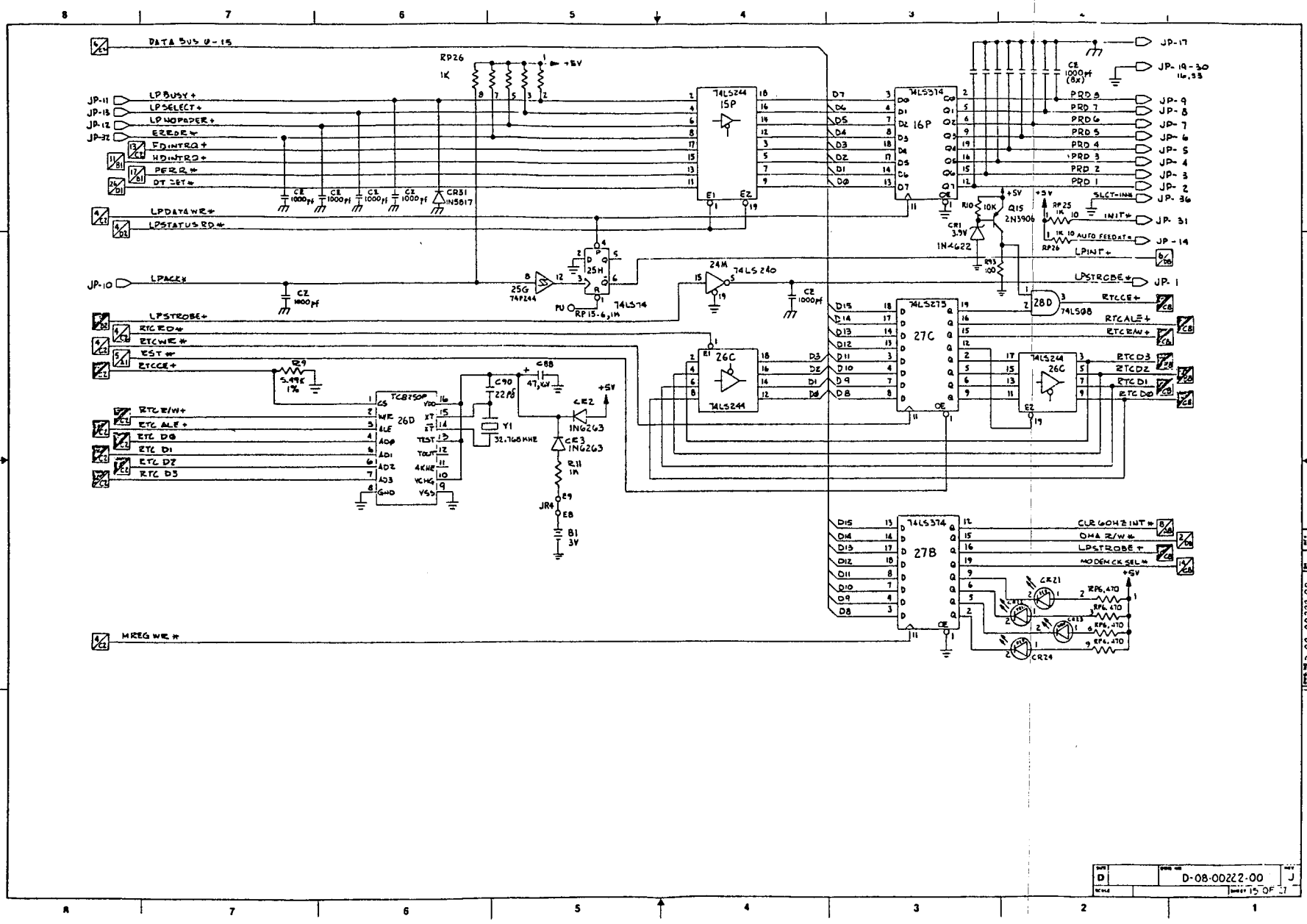
DATA BUS 0-15
LPBUSY+
LPSELECT+
LPNOPAPER+
EZERR*
FDINTRQ+
HDINTRQ+
PERR*
DT SET*
LPDATAWR*
LPSTATUSRD*
LPACK*
LPSTROBE+
RTCRD*
RTCWR*
RST*
RTCCE+
RTC R/W+
RTC ALE+
RTC D0
RTC D1
RTC D2
RTC D3
MREGWR*
RP26
1K
+5V
74LS244
15P
74LS374
16P
74LS240
74LS74
25H
74LS273
27C
26C
28D
74LS08
27B
TC8250P
26D
Y1
32.768KHZ
CR31
IN5817
Q15
2N3906
IN4622
PRD 8
PRD 7
PRD 6
PRD 5
PRD 4
PRD 3
PRD 2
PRD 1
SLCT-IN#
INIT*
AUTO FEED*
LPINT+
LPSTROBE*
RTCCE+
RTCALE+
RTCR/W+
RTCD3
RTCD2
RTCD1
RTCD0
CLR 60HZ INT*
DMA R/W*
LPSTROBE*
MODEM CK SEL*
JP-17
JP-19-30
JP-9
JP-8
JP-7
JP-6
JP-5
JP-4
JP-3
JP-2
JP-36
JP-31
JP-14
JP-1
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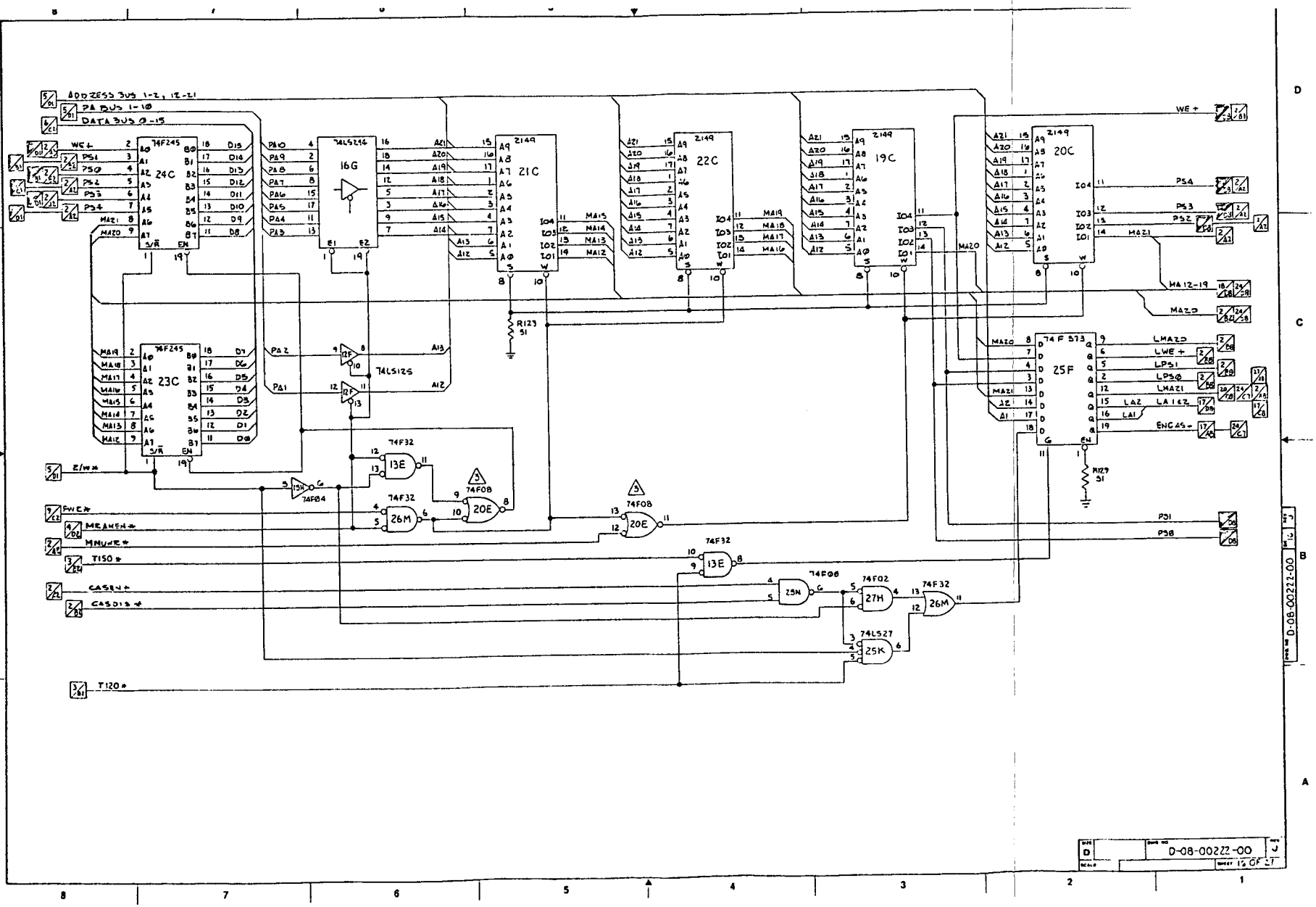
ADDRESS BUS 1-2, 12-21
PA BUS 1-10
DATA BUS 0-15
74F245
24C
74LS244
16G
2149
21C
22C
19C
20C
74F 573
25F
23C
74LS125
74F32
74F08
74F02
74LS27
13E
26M
20E
27H
25K
25N
R123 51
R129 51
WE+
PS4
PS3
PS2
MA21
MA20
MA12-19
LMA20
LWE+
LPS1
LPS0
LMA21
LA2
LA1&2
ENCAS-
E/W*
EWE*
MEAMEN*
MMUWE*
T150*
CASEN*
CASDIS*
T120*
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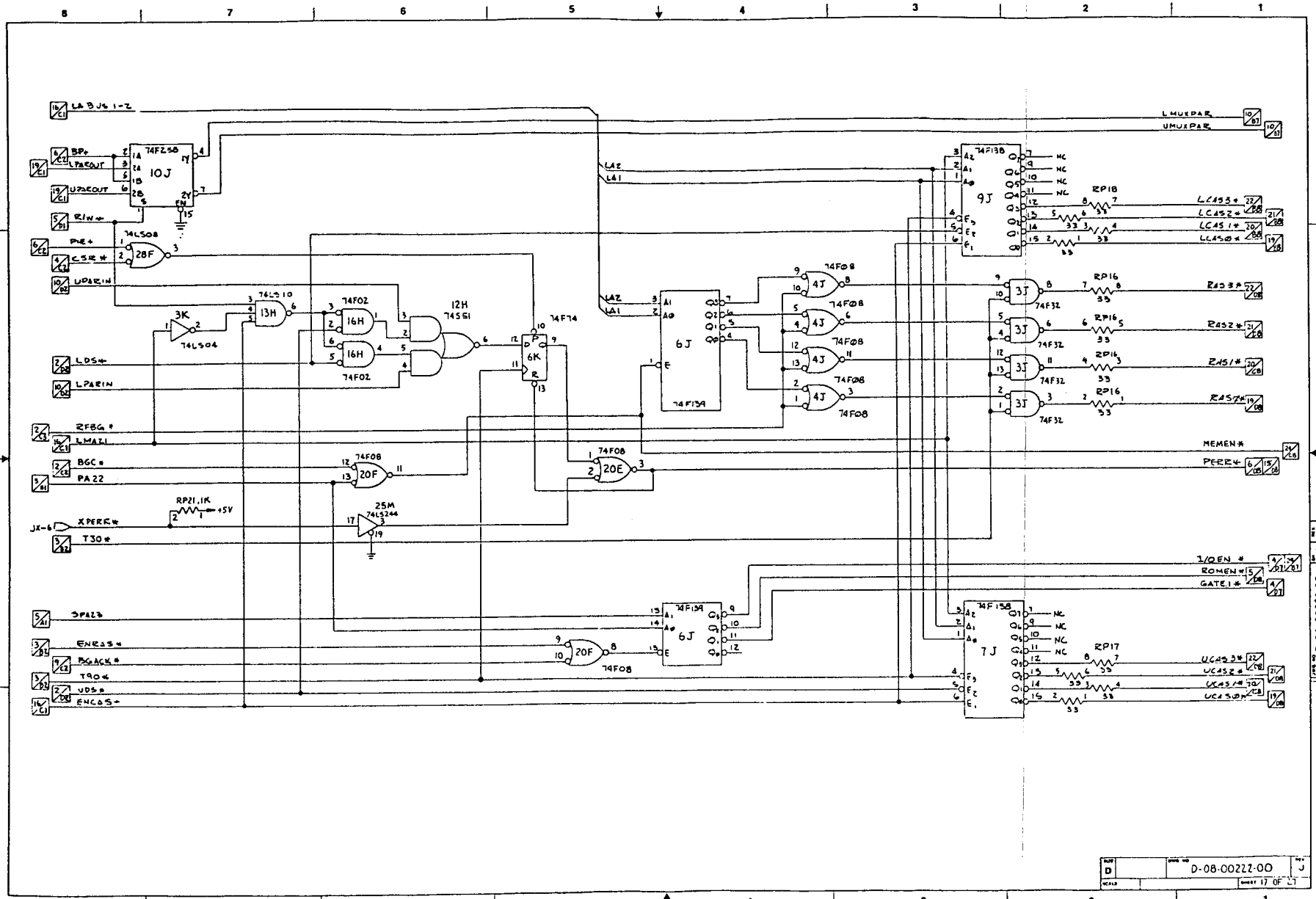
LABUS 1-Z
BP+
LPARCUT
U2ACOUT
RIN*
PHI+
CSR*
UPARIN
LDS*
LPARIN
RFBG*
LMAZI
BGC*
PA22
XPERR*
T30*
SPAZ3
ENEAS*
BGACK*
T90*
UDS*
ENCAS*
74FZ58
10J
74LS08
28F
74LS10
13H
74LS04
3K
74F02
16H
12H
74S51
74F74
6K
74F08
20F
20E
74LS244
25M
RP21.1K
+5V
74F139
6J
74F08
4J
74F32
3J
74F138
9J
7J
RP18
RP16
RP17
33
LMUXPAR
UMUXPAR
LA2
LA1
LCAS3*
LCAS2*
LCAS1*
LCAS0*
RAS3*
RAS2*
RAS1*
RAS0*
MEMEN*
PERR*
I/OEN*
ROMEN*
GATE1*
UCAS3*
UCAS2*
UCAS1*
UCAS0*
NC
D-08-00222-00
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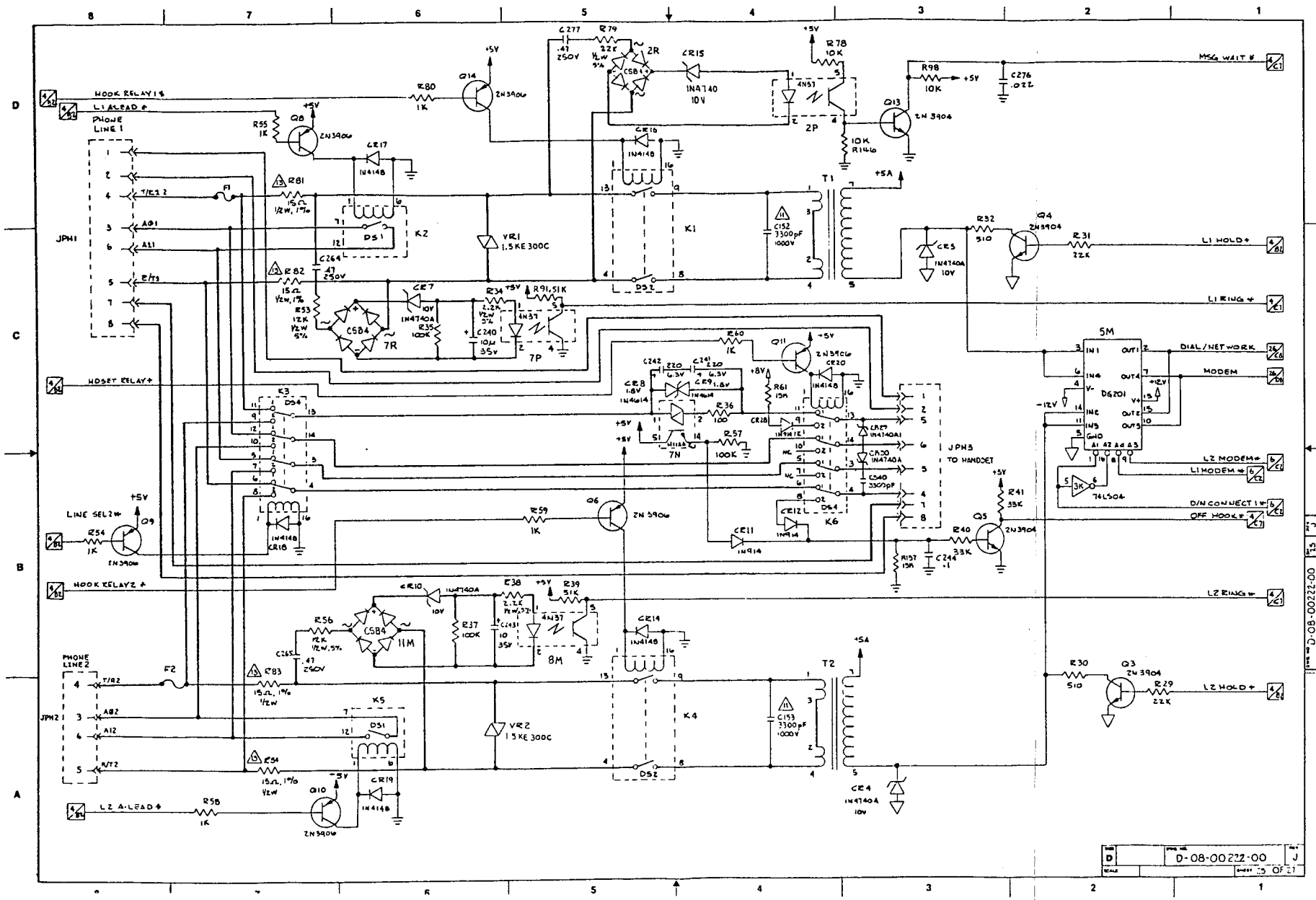
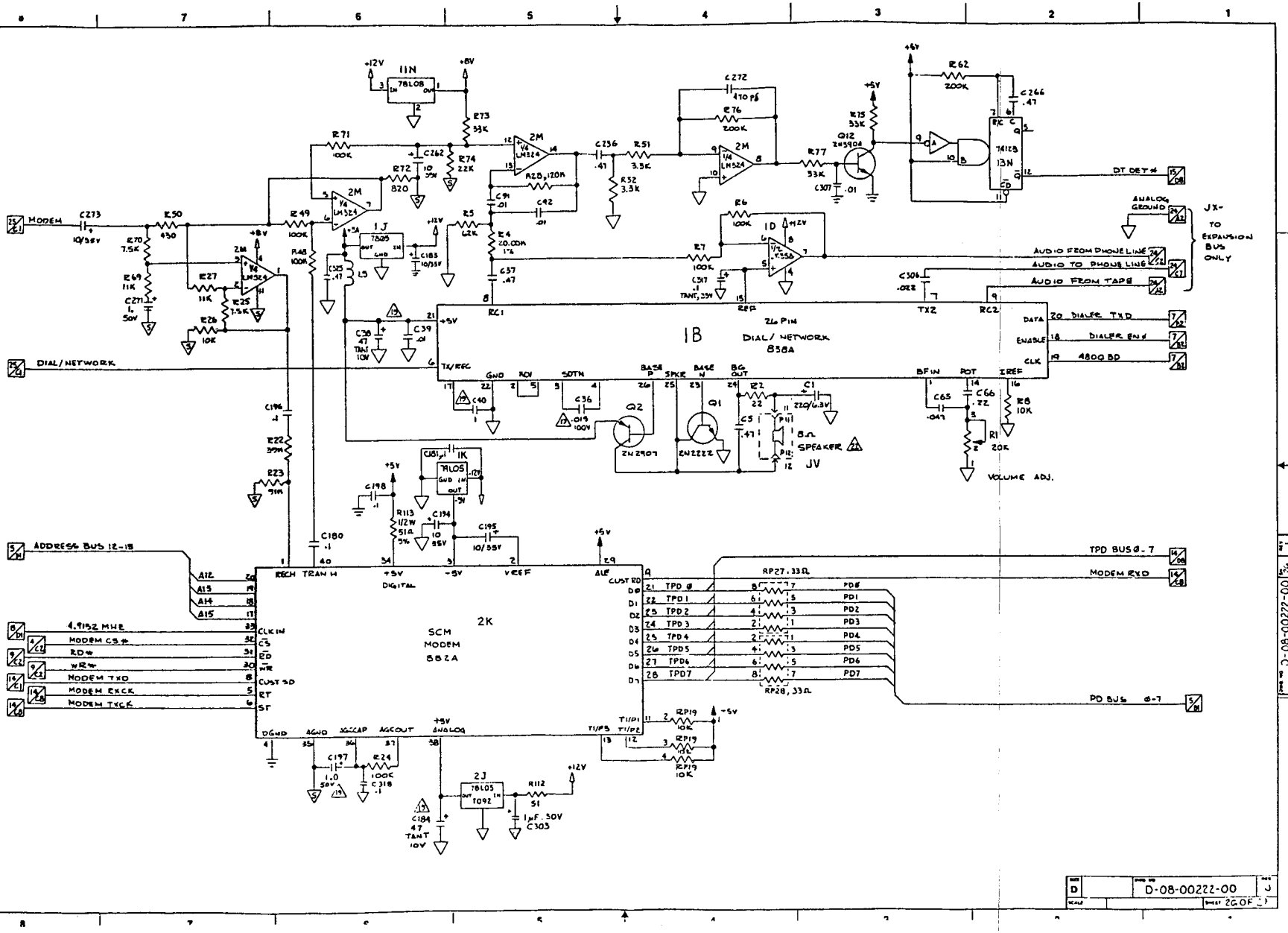

HOOK RELAY 1 ⊕
L1 A-LEAD ⊕
PHONE LINE 1
JPH1
T/R2 2
A21
A11
R/T2
F1
K2
DS1
K1
DS2
T1
+5A
VR1 1.5KE 300C
C152 3300pF 1000V
CR5 IN4740A 10V
Q4 2N3904
R32 510
R31 22K
L1 HOLD ⊕
L1 RING ⊕
MSG WAIT ⊕
R98 10K
C276 .022
Q13 2N3904
R78 10K
10K R1146
2P
CR15 IN4740 10V
C277 .47 250V
R79 22K ½W 5%
2R
CSB4
Q14 2N3906
R80 1K
Q8 2N3906
R55 1K
CR16 IN4148
CR17 IN4148
R81 15Ω 1/2W, 1%
C264 .47 250V
R82 15Ω ½W, 1%
R53 12K ½W 5%
CSB4 7R
CR7 10V IN4740A
R35 100K
R34 2.2K ½W 5%
C240 10μ 35V
4N37 7P
R91, 51K
R40 1K
Q11 2N3906
CR20 IN4148
C242 220 6.5V
C241 220 6.5V
C239 6.5V
CR8 1.8V IN4614
CR9 1.8V IN4614
+8V
R61 15M
R36 100
R57 100K
7N
CR18 IN4148
CR28 IN914
CR29 IN4740A
CR30 IN4740A
C240 3300pF
DS4
K6
CR12 IN914
CR11 IN914
JPH3 TO HANDSET
R41 33K
Q5 2N3904
R40 33K
C244 .1
MIST 15M
5M
D6201
DIAL/NETWORK
MODEM
L2 MODEM ⊕
L1 MODEM ⊕
74LS04
D/N CONNECT 1 ⊕
OFF HOOK ⊕
HOOK RELAY 2 ⊕
L2 RING ⊕
LINE SEL 2 ⊕
Q9 2N3906
R54 1K
CR10 IN4740A
R56 12K ½W, 5%
CSB4 11M
R37 100K
C238 2.2K ½W, 5%
C243 10 35V
4N37 8M
R39 51K
CR14 IN4148
PHONE LINE 2
JPH2
T/R2
A22
A12
R/T2
F2
K5
DS1
K4
DS2
T2
+5A
VR2 1.5KE 300C
C153 3300pF 1000V
CR4 IN4740A 10V
R83 15Ω, 1% 1/2W
R84 15Ω, 1% 1/2W
R30 510
Q3 2N3904
R29 22K
L2 HOLD ⊕
L2 A-LEAD ⊕
R58 1K
Q10 2N3906
CR19 IN4148
R59 1K
Q6 2N3906
HOOK RELAY 2 ⊕
HOSET RELAY ⊕
D-08-00222-00
J
SHEET 25 OF 27


1B
DIAL/ NETWORK
858A
26 PIN
2K
SCM
MODEM
882A
SPEAKER
VOLUME ADJ.
DIAL/NETWORK
MODEM
ADDRESS BUS 12-18
4.9152 MHz
MODEM CS*
RD*
WR*
MODEM TXD
MODEM EXCK
MODEM TXCK
TPD BUS 0-7
MODEM RXD
PD BUS 0-7
AUDIO FROM PHONE LINE
AUDIO TO PHONE LINE
AUDIO FROM TAPE
ANALOG GROUND
TO EXPANSION BUS ONLY
DT DET*
DATA
ENABLE
CLK
DIALER TXD
DIALER ENA
4800 BD
D-08-00222-00
2G OF

I.C. VOLTAGE CHART

DEVICE	REFERENCE DESIGNATION	+5V	DGND	PAGE NO.
74F08	22D, 25N	14	7	2,4,5,16,20,23
74F02	16H, 27H	14	7	3,4,5,16,17,24
74S03	18M	14	7	12
74LS04	3K	14	7	3,5,6,17,25
74F04	13H	14	7	2,4,12,16
74F08	4J, 28E, 28F, 24N	14	7	2,7,16,17,23,24
74LS08	28D, 28F	14	7	3,4,5,6,11,15,17
74LS10	13H	14	7	5,17
74F10	13M	14	7	12
74F11	27F	14	7	2,4
74LS14	4M, 18M	14	7	4,5,11,13,16
74F20	25C	14	7	2,23
74LS27	23D, 25K, 26M	14	7	2,6,8,16,25
74F32	3J, 13E, 21F, 24M, 24P, 26M	14	7	2,3,4,5,7,9,11,16,17,20,24
74S51	12M, 19M	14	7	3,17
74F64	18G	14	7	3
74LS74	25H, 27M, 28M	16	8	2,6,7,8,11,15
74F74	6M, 15M, 16M, 17M	14	7	4,12,17
74F86	26D	14	7	8,13,24
74S112	21E, 28G	16	8	3
74123	15N	16	8	12, 26
74S124	14N	16	9	12
74LS138	26G, 27G, 28G	16	8	4
74F138	7J, 9J	16	8	17
74LS125	12F, 26M	16	8	5,11,13,16
74F139	6J	16	8	17
74F153	14M	16	8	12
74LS157	19M, 19N	16	8	14
74F175	18D, 18H	16	8	3,8
74LS240	17M, 24M	20	10	4,13,15
74LS244	9M, 15P, 16G, 24F, 25M, 26C	20	10	2,4,5,6,13,15,16,17,24
74F244	16F, 17F, 19G, 22B, 25G	20	10	2,3,5,13,18,24
74F245	12C, 12D, 13A, 13C, 13D, 17B, 19B, 28D, 21B, 23B, 23C, 24B, 24C	20	10	5,8,16,20,23
74F258	18J, 11B, 11C, 11D, 11F, 11G, 11H, 12A, 12E, 19F	16	8	3,17,18
74LS259	7M, 18M	16	8	4,6
74S260	27N	14	7	3
74LS273	17M, 27C	20	10	11,13
74S299	14B, 15D	14	7	8
74LS348	18F	16	8	6
74LS373	16D, 18C, 21D, 24D, 25D	20	10	6
MF373	17G, 25F	20	10	5,16
74F374	16M	20	10	2,3,6,12
74LS374	16P, 27B	20	10	15
74LS393	16E, 20D	14	7	7
74LS32	26F	14	7	4,5,8

I.C. VOLTAGE CHART

DEVICE	REFERENCE DESIGNATION	+5V	DGND	PAGE NO.
26LS31	14H	16	8	6,12
26LS32	13M	16	8	12
1488	22P ⚠E		7	14
1489	18P, 28P	14	7	14
2149	19C, 28C, 21C, 22C	18	9	16
2764/128	14C, 15C	28	14	5
6850	15G	12	1	14
4416	14A, 15A, 16A, 17A	5	18	8
4864	2A, 3A, 4A, 5A, 6A, 7A, 8A, 9A, 10A, 2B, 3B, 4B, 5B, 6B, 7B, 8B, 9B, 10B, 2C, 3C, 4C, 5C, 6C, 7C, 8C, 9C, 10C, 2D, 3D, 4D, 5D, 6D, 7D, 8D, 9D, 10D, 2E, 3E, 4E, 5E, 6E, 7E, 8E, 9E, 10E, 2F, 3F, 4F, 5F, 6F, 7F, 8F, 9F, 10F, 2G, 3G, 4G, 5G, 6G, 7G, 8G, 9G, 10G, 2M, 3M, 4M, 5M, 6M, 7M, 8M, 9M, 10M	8	16	13,20,21,22
68B18	14E	14/19	6,33	5
8086	1B			26
8088	2A			26
7281	21M	40	20	14
C581	2A, 7A, 11M			23
DG281	5M			23
HI1AA2	7N			23
LM324	2M			26
LM358	1D			26
LF412	17N			12
AN37	2P, 7P, 8M			23
PAL16L8A	24G	20	10	2
PAL16R4	14M	20	10	12
PAL16R4A	24M	20	10	2
PAL16R8A	25B	20	10	2
1C8Z50P	26D	N/A	8	15
WD1010-05	21M	40	20	11
WD2797	22M	21	20	12
75L05	1K			26
1805	1J			26
75L08	11N			26
75L05	2J			26
VIDEO ARRAY	17C	40	20	7
DMA DATA ARRAY	22M	20	40	10
DMA ADDRESS ARR	22E	20	40	9

A PAL Equations

The **UNIX** PC uses four programmable array logic (PAL) integrated circuits: the disk, arbitor, and memory management unit PALs are shown on sheet 2; the data separator PAL is shown on sheet 12.

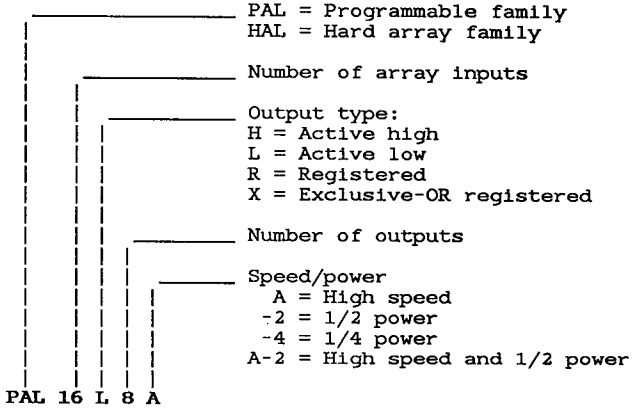
The operation of a PAL is described by a logic equation in a PAL listing. The listing is used to determine the correct logic levels of the outputs with a given set of inputs.

PROM's have been widely used by system designers to implement firmware. The PAL extends this programmable flexibility by utilizing fusible link technology to implement logic functions.

The PAL implements the familiar sum of products logic by using a programmable AND array whose outputs feed a fixed OR array. Since the sum of products form can express any Boolean transfer function, the PAL circuit uses are limited only by the number of terms available in the AND/OR arrays. PALs come in different sizes to allow for effective logic optimization.

PALs can be programmed in most standard PROM programmers with the addition of a PAL personality card.

The PAL identification number is broken down as follows:



PAL Equations

Arbitor: PAL 16R8A (Sheet 2: C-6)

Pin Signal Names

Pin Number	Mnemonic	Description
1	PCK*	Input: processor clock
2	RFRQ*	Input: refresh request
3	EXP3RQ*	Input: expansion board 3 request
4	DKRQ*	Input: disk bus request
5	EXP2RQ*	Input: expansion board 2 request
6	EXP1RQ*	Input: expansion board 1 request
7	EXP0RQ*	Input: expansion board 0 bus request
8	BGACK*	Input: bus grant acknowledge
9	ENRAS*	Input: enable row address strobe
10	(Ground)	------
11	OE	Output enable
12	NRF/BGC*	Output: nonrefresh/bus grant common
13	BGC*	Output: bus grant common (any bus master except 68010)
14	EXP0BG*	Output: expansion board 0 bus grant
15	EXP1BG*	Output: expansion board 1 bus grant
16	EXP2BG*	Output: expansion board 2 bus grant
17	DKBG*	Output: disk drive bus grant
18	EXP3BG*	Output: expansion board 3 bus grant
19	RFBG*	Output: refresh bus grant
20	VCO	Voltage-controlled oscillator: +5v

NOTATION

XX	Boolean AND
*	Negation or active low
:=	Register output latched clock
+	Boolean OR

EQUATIONS FOR BUS GRANT

DKBG := (DKRQ X ENRAS* X BGACK* X DKRQ*) + EXP3BG X BGACK)

```
RFBG    := (RFRQ X ENRAS* X BGACK* X DKRQ* X EXP3RQ*)
           + (RFBG X BGACK)

EXP2BG  := (EXP2RQ X ENRAS* X BGACK* X DKRQ* X EXP3RQ* X RFRQ*)
           + (EXP2BG X BGACK)

EXP1BG  := (EXP1RQ X ENRAS* X BGACK* X DKRQ*  X EXP3RQ* X RFRQ*
           X EXP2RQ*) + (EXP1BG X BGACK)

EXP0BG  := (EXP0RQ X ENRAS* X BGACK* X DKRQ* X EXP3RQ* X RFRQ* X
           EXP2RQ* X EXP1RQ*) + (EXP0BG X BGACK)
```

The six preceding logic equations describe the input conditions that produce a DMA bus grant in response to a request from any one of the six devices that requests the bus. The devices are named by the output expression. The equations are listed in order of priority: DKRQ (disk request) is the highest priority; EXP0 (expansion board 0) is the lowest. The 68010 does not appear in these equations, because it receives the bus only when no DMA device is requesting the bus. To the right of the equals sign in each logic equation are four terms in the following form:

```
[bus grant] = [bus request] X [bus not in use] X [priority term]
           + [latch term]
```

The first term is the bus request (RFRQ, EXP3RQ, DKRQ, etc.). This term is ANDed with ENRAS* and BGACK*, which form the "bus not in use" term. The result is that, if a bus cycle is in process when a request is made, the bus grant is not issued until the current cycle is completed.

The third term is the priority term. In the equation for EXP3BG, the priority term is DKRQ*, because disk request has a higher priority than expansion board 3. Thus the bus is not granted to expansion board 3 if a refresh request is pending. Each equation has a priority term that names all the devices of higher priority. The first equation for DKBG has no priority term, because there is no device of higher priority. The last equation for expansion board 0 has a priority term that names all devices that may request the bus except itself, since it is the lowest priority. Thus the bus is not granted for a given line if any one of those above is pending.

The fourth term is the latch term, which contains the output of the expression ANDed with bus grant acknowledge. When a bus request is granted, bus grant acknowledge keeps the bus grant active after the bus request is removed. The grant is removed when bus grant acknowledge is removed.

Equation for Bus Grant Common

```
BGC := (RFRQ + EXP3DRQ + DKRQ + EXP2RQ + EXP1RQ + EXP0RQ) X
       (ENRAS* X BGACK*) + BGC X BGACK

[bus grant common] = [any DMA request] X [bus not in use]
       + [latch]
```

This equation has the four parts shown above. The first part of this equation contains all the possible DMA devices that could request the bus ANDed with the "bus not in use" term, enable row address strobe, and bus grant acknowledge. Thus, when any DMA device requests the bus, BGC is asserted as soon as the cycle being executed is completed. Completion of the cycle is indicated when ENRAS* and BGACK* are not asserted.

The third term is a latch term consisting of the function output, BGC, ANDed with BGACK. Once the BGC is asserted, it remains asserted as long as the bus grant acknowledge is asserted, and it is deasserted when bus grant acknowledge is deasserted.

Equation for Nonrefresh Bus Grant Common

```
NRFBGC := (EXP3RQ + DKRQ + EXP2RQ + EXP1RQ + EXP0RQ) X (ENRAS* X
       BGACK* X RFQR*) + (NRFBGC X BGACK)
```

This nonrefresh bus grant is similar to bus grant common. It becomes active at the end of the current cycle when any DMA device, except refresh, requests the bus.

The last term is again a latch term to keep the bus grant active while the acknowledge is active after the original request becomes inactive.

Disk Interface: PAL 16R4A (Sheet 2: D-6)

Pin Number	Mnemonic	Description
1	1PCK+	Input: processor clock
2	RD*	Input: read--indicates 68010 or DMA device is reading memory or an I/O device
3	WR*	Input: write--indicates 68010 or DMA device is writing to memory or an I/O device
4	DMAR/W*	Input: direct memory access read/write--high indicates RAM memory is being read; low indicates RAM memory is being written
5	FDDRQL	Input: floppy disk drive data request--latched data from floppy disk controller pin 38 DRQ (data request); indicates that the floppy disk controller data register contains assembled data when a sector of the disk is being read or that it is empty during a sector write operation
6	HDBCS*	Input: hard disk buffer chip select--connected to pin 1 of hard disk controller; active low used to enable reading or writing data from the bus interface when controller data buffer is ready to transfer a byte
7	FDCS*	Input: floppy disk chip select--asserted when the 68010 is writing or reading the floppy disk controller data register
8	HDRE*	Input: hard disk read--asserted when the hard disk controller is reading a byte from the bus interface unit during a Sector Write command or when the 68010 is reading data from the disk controller data register; connected to the hard disk controller pin 6

Pin Number	Mnemonic	Description
9	HDWE*	Input: hard disk write--asserted when the hard disk controller is writing a byte to the bus interface unit during a Sector Write command or when the 68010 is writing data from the disk controller data register; connected to the hard disk controller pin 7
10	GND	Ground
11	OE	Output enable: connected low through a 330-ohm resistor to ground
12	FDRE*	Output: floppy disk read--connected to the RE pin 4 of the floppy disk controller
13	FDWE*	Output: floppy disk write--connected to the WE pin 2 of the floppy disk controller
14	FDTFER*	Output: floppy disk transfer--not connected outside of PAL used by rest of PAL logic to produce floppy disk read and write on pins 12 and 13 described above
15	QB*	Output: latch B output--not connected outside PAL chip used internally to latch status of FDTFER
16	QC*	Output: latched value of QB--not connected outside of PAL
17	QD*	Output: latched value of QC--not connected outside of PAL
18	TFER*	Output: transfer request--goes to disk DMA bus interface unit; initiates transfer of data from disk controller to bus interface unit and generates a disk bus request
19		Output: not used
20	VCC	+5 volts

LOGIC EQUATIONS

```
FDTFER    := (FDDRQL X FDTFER*) + (FDTFER X QD*)

QB        := FDTFER

QC        := QB

QD        := QC

FDRE      := (FDCS X RD) + (FDTFER X DMARW)

FDWE      := (FDCS X WR) + (FDTFER X DMARW*)

TFER      := (QD X DMARW*) + (QD* X DMARW) + QB + (HBCS X HDRE)
               + (HBCS X HDWE)
```

The transfer request (TFER) is asserted when the hard disk controller or the floppy disk controller is ready to transfer a byte to or from its data register to or from the disk bus interface unit buffers. On every other assertion of TFER, a disk DMA bus request is issued by the interface unit.

MMU and Bus Error: PAL 16L8A (Sheet 2: C-6)

Pin Number	Mnemonic	Description
1	PA22	Input
2	KADDR	Input: kernal access address, A19 A20, and A21 all low
3	SUP+	Input: 68010 in supervisor mode
4	BGC*	Input: bus grant common
5	LPS0*	Input: latched page status bit 0
6	LPS1*	Input: latched page status bit 1
7	R/W*	Input: high = read; low = write
8	LWE+	Input: latched page status bit write enable
9	SPA23	Input: highest address bit
10	GND	Ground
11	T90	Input
12	CASDIS*	Output
13	IODTACK*	Input
14	PAS*	Input
15	BERREN	Output: bus error enable
16	PGF*	Output: page fault
17	MMUERR*	Output: memory management unit error
18	UIE*	Output: user access to address outside memory
19	PPS0	Output: updated processor page status bit 0
20	VCC	+5 volts

Memory Management Unit Error Equation

```
MMUERR    =    BGC* X PA22* X SPA23* X LPS0* X LPS1*
               + BGC X LPS0* X LPS1*
               + BGC* X SUPV* X SPA23* X PA22* X KADDR
               + BGC* X SUPV* X  PA23* X PA22* X RW X LWE*
```

This equation is the logical ORing of four terms, each of which causes a memory management error.

In the first term, BGC*, PA22*, and SPA23* all high indicate a user access to RAM memory. LPS0* and LPS1* both high indicate that the access is to a page that has been designated not physically present.

In the second term, BGC high indicates a DMA access, and LPS0* and LPS1* indicate access is to a page not physically present.

In the third term, SUPV* indicates a user access, 68010 not in supervisory mode, and KADDR indicates the access is to the kernel.

In the fourth term, LWE* indicates the access is to a page not write enabled, and WE* indicates a write cycle.

The four conditions that generate a memory management error are summarized in the following table:

- Processor access to a page not present
- DMA access to a page not present
- User access to the kernel
- User attempt to write to a page not write enabled

MMUERR is used on sheet 6 to generate a level 7 interrupt.

Page Fault Equation

```
PGF  =    BGC* X PA22 X SPA23* X LPS0* X LPS1*
          + (BGC X LPS0* X LPS1*)
```

Page fault is the ORing of two terms. In the first, BGC* indicates a 68010 access, and LPS0* and LPS1 indicate access is to a page not present. In the second, BGC indicates a DMA access. Thus page fault occurs when either the 68010 or a DMA device tries to access a page not present.

User Nonmemory Location Error Equation

```
UIE = (BGC* X SUPV* X ENRAS * X PA22) + (BGC* X SUPV* X ENRAS*)
```

In this equation, SUPV* indicates a user access; PA22 and ENRAS* indicate that the access is to a nonmemory location.

Bus Error Enable Equation

```
BERREN=   BGC* X PA22* X SPA23* X LPS0* X LPS1* X T90 X PAS
        + BGC* X SUPV* X SPA23* X PA22* X KADDR X T90 X PAS
        + BGC* X SUPV* X SPA23* X PA22* X RW X LWE* X T90
        + BGC* X SUPV* X  SPA23*X PA22 X IODTACK
        + BGC* X SUPV* X SPA23* X DTACK
```

This equation is the ORing of five terms. The condition to assert each term is:

- User access to page not present
- User access to kernel
- User access to page not write enabled
- User access to address not in memory
- User access to address not in memory

BERREN is ANDed with EE* (the error enable bit) and connected to BERR- pin 22 of the 68010.

Column Address Disable Strobe Equation

```
CASDIS =  BGC* X PA22* X SPA23* X LPS0* X LPS1* X RW
        + BGC X LPS0* X LPS1* X RW
        + BGC* X SUPV* X SPA23* X PA22* X KADRR X RW
        + BGC* X SUPV* X SPA23* X PA22* X RW X LWE* X RW
```

The column disable bit prevents writing to RAM memory during a memory management unit error. Thus the terms of these equations contain the same conditions that generate the MMUERR ANDed with the RW write bit.

Page Status Bit 0 Equation

```
PPS0 =    RW* X LPS1* X LPS0 X MMUERR*
        + RW* X LPS1 X LPS0* X MMUERR*
        + LPS0* X MMUERR
```

This equation lists the following three conditions for setting bit 0 of page status to 1:

- Writing to a page that is present but has never been written to, when there is no MMUERR

- Writing to a page that is present and has been read but not previously written to, when there is no MMUERR
- A MMUERR exists and PSO was previously written to, when there is no MMUERR
- A MMUERR exists and PSO was previously 0.

Hard Disk Data Separator: PAL 16R4 (Sheet 26)

Pin Number	Mnemonic	Description
1	MUXCLK*	Input clock for multiplex clock output
2	PLLCLK	Output of VCO
3	DATA0	Data and clock from drive 0
4	DATA1	Grounded
5	DDRIVE0*	Grounded
6	HDRGATE	High when disk controller is inspecting data
7	PCLK*	10 MHz
8	TEST	Grounded
9	REF	Grounded
10	GND	
11	OE*	Grounded
12	RCLK	1/2 PLL
13	DCLK	No external connection
14	FFA*	No external connection
15	OSCENB*	Enables VCO
16	FFB*	No external connection
17	FFC*	No external connection
18	CLR*	Clears pullup/pulldown flipflops
19	MUX*	Multiplex clock output
20	VCC	

Equations

```
FFA     :  =    HDRGATE

FFB     := FFA

FFC     := FFB

OSCENB := HDRGATE* FFC* + HDDRGATE X FFC

CLR      = HDRGATE* X FFC + HDRGATE X FFC* + OSCENB*

DCLK*    = PLLCLK X RCLK + PLLCLK* X DCLK* + RCLK X DCLK* + TEST
```

RCLK* = PLLCLK* X DCLK* + PLLCLK X RCLK* + DCLK* X RCLK*

MUX = HDRGATE X DATA0* X DDRIVE0 + HDRGATE X DATA1*
X DDRIVE0* + HDRGATE* X PCLK*

If HDRGATE is high, MUX pin 19 outputs drive 0 data coming in on pin 3. If HDRGATE is low, MUX outputs PCK* coming in on pin 7.

When HDRGATE is high, PLLK is phase-locked to DATA0 at pin 3 at twice the frequency. DATA0 is 5 MHz and PLL is 10 MHz.

When HDRGATE is low, PLLK is 10 MHz, phase locked to PCK* at pin 7.

RCLK is always half the frequency of PLLCLK.

B Mnemonics

Mnemonic	Description
A	
A1-A23	System address bits
ABUS	System address bus
ADX	Address
ARB	Bus arbitor
AUTO FEEDXT	Automatic line feed
B	
BCS	Buffer chip select
BERR	Bus error
BERREN	Bus error enable
BGACK	Bus grant acknowledge
BGC	Bus grant common
BGCAK	Bus grant common acknowledge
BM WINDOW	Bit map window
BMACK	Bit map acknowledge
BMCAS	Bit map column address strobe
BMRAS	Bit map row address strobe
BMR/W	Bit map read/write
BMSEL	Bit map select
BP	Bad parity
BRABUS 0-7	Bit map RAM address bus
BSR0RD	Bus status register 0 read
C	
CAS	Column address strobe
CASDIS	Column address strobe disable
CASEN	Column address strobe enable
CCK	Character clock
CD	Carrier detect
CLR 60HZ INT	Clear 60-Hz interrupt
CLRREADD	Clear refresh address
CO	Carryout
COMMOSC	Communications oscillator
CPU	Central processing unit
CS	Chip select
CSR	Clear status register
CTS	Clear to send

D

D0-D15	System data bits
DADDWR	Direct memory access address counter write
DATAIN	Data in
DBLDEN	Double density
DBUS	System data bus
DCNTCS	Direct memory access word counter chip select
DCS	Disk controller select
DD	Disk data bus
DDBUS 0-7	Disk data bus 0-7
DDRIVE0	Disk drive 0
DFAULT	Data fault
DIALER EN	Dialer enable
DIALER TXD	Dialer transmit data
DINDEX	Disk index pulses
DISPEN	Display enable
DKBG	Disk bus grant
DKBGA	Disk bus grant acknowledge
DKRQ	Disk bus request
DMA	Direct memory access
DMAEN	Direct memory access enable
DMAR	Direct memory access read
DMAR/W	Direct memory access read/write
D/N CONNECT 1	Dial network connected to line 1
DREADY	Drive ready
DRQ	Data request
DRUN	Data run
DSCOMPL	Disk seek complete
DSR	Data set ready
DT DET	Dial tone detect
DTACK	Data transfer acknowledge
DTRK 0	Disk track 0

E

EE	Error enable
EN	Enable
ENCAS	Enable column address strobe
ENRAS	Enable row address strobe
EXP0-3BG	Expansion board 0-3 bus grant
EXP0-3RQ	Expansion board 0-3 request

F

FC	Function code
FDCS	Floppy disk chip select
FDDRIVE0	Floppy disk drive 0
FDDRQ	Floppy disk data request
FDDRQL	Floppy disk data request latched
FDINDEX	Floppy disk index
FDINTRQ	Floppy disk interrupt request
FDMOTOR	Floppy disk motor enable
FDPRESENT	Floppy disk present
FDRD	Floppy disk read
FDRE	Floppy disk read enable
FDREADY	Floppy disk ready
FDRST	Floppy disk reset
FDTRACK 0	Floppy disk track 0
FDWE	Floppy disk write enable
FDWPRT	Floppy disk write protect
FF	Flipflop
FWR	Fast write

G

GCRWR	General control register write
GND	Ground
GSR	General status register
GSRRD	General status register read

H

HAL	Hard array of logic
HDBCS	Hard disk buffer chip select
HDBRDY	Hard disk buffer ready
HDCS	Hard disk chip select
HDCTRLWR	Hard disk controller write
HDINTRQ	Hard disk interrupt request
HDL	Head load
HDRE	Hard disk read enable
HDRST	Hard disk reset
HDSEL0-2	Head select bits 0-2
HDSETRELAY	Handset relay
HDWDATA	Hard disk write data
HDWE	Hard disk write enable
HSYNC	Horizontal synchronization

I

ID	Identify
IDMAR/W	Identify DMA read/write operation
INIT	Centronics reset and initialize control signal
INT	Interrupt
INTA	Interrupt acknowledge
INTRQ	Interrupt request
I/O DTACK	I/O data transfer acknowledge
I/OEN	I/O enable
I/ORQ	I/O request
IPL	Interrupt priority level

K

KADDR	Kernel address
KBEN	Keyboard enable
KBINT	Keyboard interrupt
KBRST	Keyboard reset
KBRXD	Keyboard receive data
KBTXD	Keyboard transmit data

L

L1 A-LEAD	Line 1 A-lead
L1 HOLD	Line 1 hold
L1 MODEM	Line 1 modem
L1 RING	Line 1 ring
L2 A-LEAD	Line 2 A-lead
L2 HOLD	Line 2 hold
L2 MODEM	Line 2 modem
L2 RING	Line 2 ring
LA	Latched address
LA BUS	Local address bus
LBERR	Latched bus error
LCAS	Lower column address strobe
LDS	Lower data strobe
LINE SEL2	Line select 2
LMA	Latched map address
LMUXPAR	Lower multiplexed parity
LPACK	Line printer acknowledge
LPARIN	Lower parity interrupt
LPAROUT	Low parity output

L (continued)

LPBUSY	Line printer busy
LPDATAWR	Line printer data write
LPINT	Line printer interrupt
LPNOPAPER	Line printer out of paper
LPS	Latched page status
LPSELECT	Line printer select
LPSTATUSRD	Line printer status read
LPSTROBE	Line printer strobe
LWE	Latched write enable

M

MA	Mapped address
MA BUS	Mapped address bus
MCK	Modem clock
MCKSEL	Modem clock select
MEMEN	Memory enable
MFM	Modified frequency modulation
MMU	Memory management unit
MMUERR	Memory management unit error
MMUWR	Memory management unit write
MMUWREN	Memory management unit write/read enable
MMUWREND	Memory management unit write/read enable data
MODEM CK SEL	Modem clock select
MODEM RXCK	Modem receive clock
MODEM RXD	Modem receive data
MODEM TXCK	Modem transmit clock
MODEM TXD	Modem transmit data
MODEMCS	Modem chip select
MOSEN	Processor data transceiver enable
MPU	Microprocessing unit
MRAEN	Map RAM enable
MRAMEN	Map RAM enable
MREG WR	Miscellaneous control register write
MSG WAIT	Message waiting
MW	Memory write

N

NMI	Nonmaskable interrupt
NPC	Nonprocessor cycle
NRFBGC	Nonrefresh bus grant common

O

OSCENB	Oscillator enable

P, Q

PA BUS	Processor address bus
PAL	Programmable array of logic
PAS	Processor address strobe
PCK	Processor clock
PCLK	Processor clock
PD	Pumpdown
PD BUS	Processor data bus
PF	Page fault
PIE	Parity interrupt enable
PRD1-8	Line printer data bits

R

RAMEN	RAM enable
RAS	Row address strobe
RD	Read
RFBG	Refresh bus grant
RFRQ	Refresh bus request
ROMEN	Read only memory enable
RTCALE	Realtime clock address latch enable
RTCD0-4	Realtime data bits
RTCLE	Realtime clock latch enable
RTCR/W	Realtime clock read/write
R/W	Read/write

S

SUPV	Supervisory mode

T

T30-T120	Memory timing delay outputs in nanoseconds
TFER	Transfer request
TPD0-7	Serial controller data bus

U, V

UCAS	Upper column address strobe
UDS	Upper data strobe
UIE	User interrupt error
U/OERR	Disk DMA underrun or overrun error

W

WE	Write enable
WR	Write

X, Y, Z

XI/O EN	Expansion I/O enable
XPERR	Expansion parity error

C Expansion Memory Locations

This appendix is a table listing the possible memory configurations for the **UNIX** PC.

The columns of the table are labeled as follows:

- Total System Memory - This is the total amount of Random Access memory (RAM) on the machine including on-board (CPU) memory and expansion memory.
- CPU On-Board Memory - This is the amount of RAM on the **UNIX** PC main sytem board.
- Expansion Memory Slot 1 - This is the first **UNIX** PC expansion slot. Facing the rear of the machine, it is located on the left side as shown in Figure 1.
- Expansion Memory Slot 2 - This is the second **UNIX** PC expansion slot. Facing the rear of the machine, it is the middle slot as shown in Figure 1.
- Expansion Memory Slot 3 - This is the third **UNIX** PC expansion slot. Facing the rear of the machine, it is located on the right as shown in Figure 1.

The table also uses the following mnemonics:

MNEMONIC	MEANING
*	Empty slot or I/O card without memory
0.5 CPU	**UNIX** PC equipped with 0.5MB of on-board RAM
1.0 CPU	**UNIX** PC equipped with 1.0MB of on-board RAM
2.0 CPU	**UNIX** PC equipped with 2.0MB of on-board RAM
0.5 RAM	0.5MB RAM Expansion Board
2.0 RAM	2.0MB RAM Expansion Board
0.5 EIA	EIA/RAM Combo Board with 0.5MB of RAM
1.0 EIA	EIA/RAM Combo Board with 1.0MB of RAM
1.5 EIA	EIA/RAM Combo Board with 1.5MB of RAM

How to Use this Table

The table is organized according to the total amount of memory the system will have after installing additional memory cards. The following examples illustrate how to use the table.

1. You have a **UNIX** PC with 0.5MB of on-board memory and you want to install a 0.5MB memory expansion board, bringing the total memory to 1.0MB. First look in the Total System Memory column for 1.0MB. Then, locate the corresponding amount of on-board memory in the next column, in this case 0.5MB. Next, look at the last three columns. You'll see that you can put your 0.5MB RAM board in expansion slot 1, 2, or 3.

2. If you want to install a second 0.5MB RAM expansion board, bringing your systems total memory to 1.5MB, you would look in the Total System Memory column for 1.5MB. Then, you would look for the same amount of on-board memory, or 0.5MB. Next, you would look at the last three columns to see where you can place the additional expansion card. In this case, the two 0.5MB RAM cards have to be placed in either expansion slots 1 and 2, or in slots 2 and 3. You cannot place them slots 1 and 3.

Expansion Memory Locations				
TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
0.5 MB	0.5 CPU	*	*	*
1.0 MB	0.5 CPU	0.5 RAM * *	* 0.5 RAM *	* * 0.5 RAM
		0.5 EIA * *	* 0.5 EIA *	* * 0.5 EIA
	1.0 CPU	*	*	*
1.5 MB	0.5 CPU	0.5 RAM *	0.5 RAM 0.5 RAM	* 0.5 RAM
		0.5 EIA *	0.5 RAM 0.5 RAM	* 0.5 EIA
		1.0 EIA * *	* 1.0 EIA *	* * 1.0 EIA
	1.0 CPU	0.5 RAM * *	* 0.5 RAM *	* * 0.5 RAM
		0.5 EIA * *	* 0.5 EIA *	* * 0.5 EIA

Expansion Memory Locations

Expansion Memory Locations (Continued)				
TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
2.0 MB	0.5 CPU	0.5 RAM	0.5 RAM	0.5 RAM
		0.5 RAM	0.5 RAM	0.5 EIA
		1.0 EIA *	* 1.0 EIA	0.5 RAM 0.5 RAM
		0.5 EIA 0.5 EIA 1.0 EIA * 1.0 EIA *	1.0 EIA * 0.5 EIA 0.5 EIA * 1.0 EIA	* 1.0 EIA * 1.0 EIA 0.5 EIA 0.5 EIA
		1.5 EIA * *	* 1.5 EIA *	* * 1.5 EIA
	1.0 CPU	0.5 RAM *	0.5 RAM 0.5 RAM	* 0.5 RAM
		0.5 EIA *	0.5 RAM 0.5 RAM	* 0.5 EIA
		1.0 EIA * *	* 1.0 EIA *	* * 1.0 EIA
	2.0 CPU	*	*	*

Expansion Memory Locations (Continued)				
TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
2.5 MB	0.5 CPU	2.0 RAM * *	* 2.0 RAM *	* * 2.0 RAM
	1.0 CPU	0.5 RAM	0.5 RAM	0.5 RAM
		0.5 RAM	0.5 RAM	0.5 EIA
		1.0 EIA * 0.5 EIA 0.5 EIA 1.0 EIA * 1.0 EIA * 1.5 EIA * *	* 1.0 EIA 1.0 EIA * 0.5 EIA 0.5 EIA * 1.0 EIA * 1.5 EIA *	0.5 RAM 0.5 RAM * 1.0 EIA * 1.0 EIA 0.5 EIA 0.5 EIA * * 1.5 EIA
	2.0 CPU	0.5 RAM * *	* 0.5 RAM *	* * 0.5 RAM
		0.5 EIA * *	* 0.5 EIA *	* * 0.5 EIA

Expansion Memory Locations

Expansion Memory Locations (Continued)

TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
3.0 MB	1.0 CPU	2.0 RAM * *	* 2.0 RAM *	* * 2.0 RAM
	2.0 CPU	0.5 RAM * 0.5 RAM	0.5 RAM 0.5 RAM *	* 0.5 RAM 0.5 RAM
		0.5 RAM 0.5 RAM 0.5 EIA * *	0.5 EIA * 0.5 RAM 0.5 RAM *	* 0.5 EIA * 0.5 EIA *
		1.0 EIA * *	* 1.0 EIA *	* * 1.0 EIA
3.5 MB	2.0 CPU	0.5 RAM	0.5 RAM	0.5 RAM
		0.5 RAM	0.5 RAM	0.5 EIA
		1.0 EIA *	* 1.0 EIA	0.5 RAM 0.5 RAM
		0.5 EIA 0.5 EIA 1.0 EIA * 1.0 EIA *	1.0 EIA * 0.5 EIA 0.5 EIA * 1.0 EIA	* 1.0 EIA * 1.0 EIA 0.5 EIA 0.5 EIA

Expansion Memory Locations (Continued)				
TOTAL SYSTEM MEMORY	CPU ON-BOARD MEMORY	EXPANSION MEMORY		
		SLOT 1	SLOT 2	SLOT 3
3.5 MB (cont'd)	2.0 CPU (cont'd)	1.5 EIA * *	* 1.5 EIA *	* * 1.5 EIA
4.0 MB	2.0 CPU	2.0 RAM * *	* 2.0 RAM *	* * 2.0 RAM

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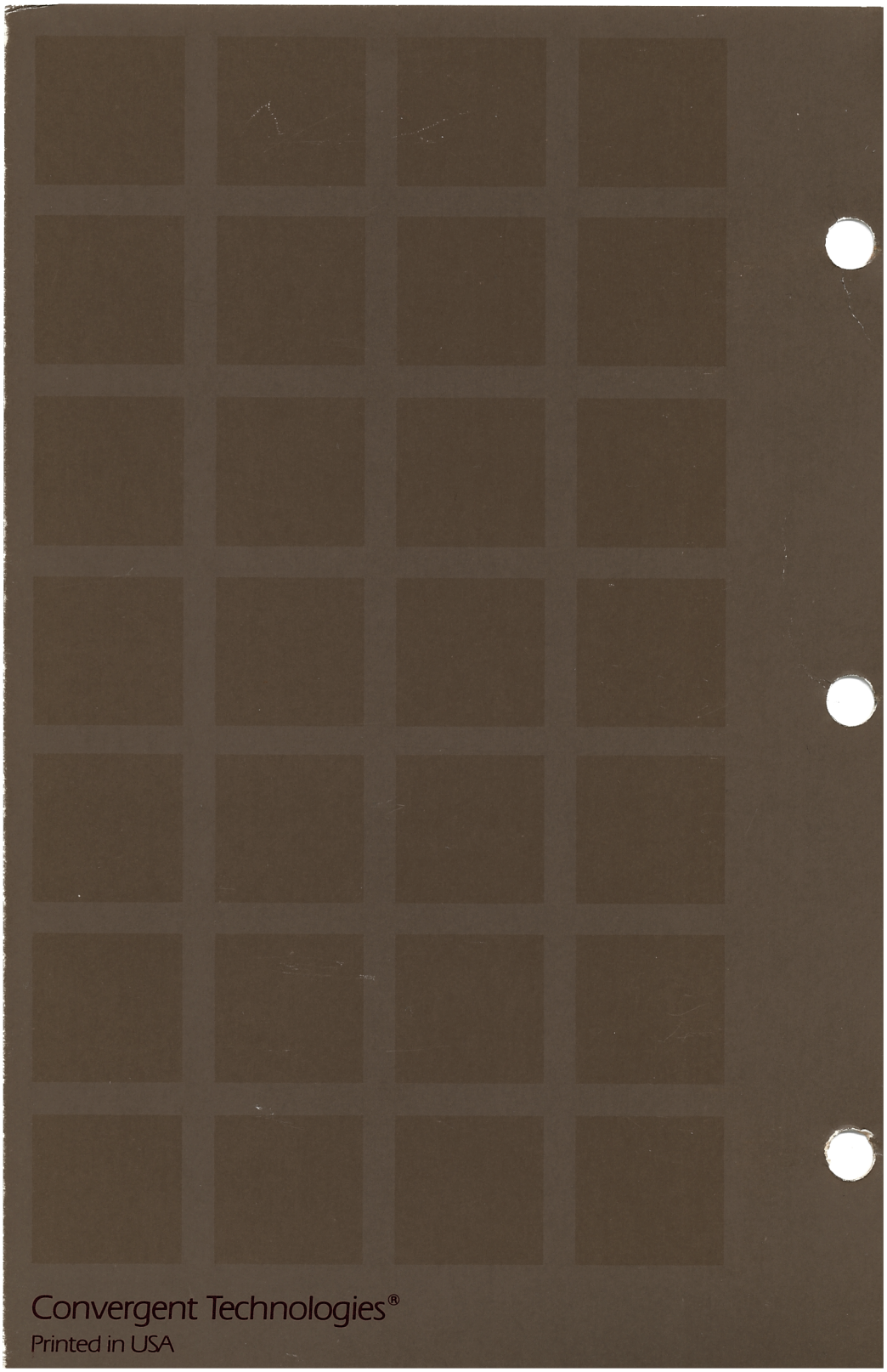
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